GreenPAK Designer User Guide

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1. Introduction

This document describes the installation and usage of Silego GreenPAK® Designer software. This software can be used as a stand-alone application for the firmware development and for GreenPAK chips programming. If the information in this guide is not sufficient to resolve issues experienced with GreenPAK Designer, refer to the resources listed under the Support section.

Features that are common for GreenPAK 1 Designer, GreenPAK 2 Designer, GreenPAK 3 Designer and GreenPAK 4 Designer are described in chapters with a GreenPAK Designer general name. The differences are described in separate chapters.

1.1 Application Overview

Each GreenPAK Designer (GreenPAK 1 Designer, GreenPAK 2 Designer, GreenPAK 3 Designer and GreenPAK 4 Designer) is a full-featured integrated development environment (IDE) that allows you to specify exactly how you want the device to be configured. This provides you direct access to all GreenPAK device features and complete control over the routing and configuration options. GreenPAK Designer will be used as a general name for GreenPAK 1 Designer, GreenPAK 2 Designer, GreenPAK 3 Designer and GreenPAK 4 Designer.

GreenPAK Designer has an integrated programming tool that allows you to program configured design into your GreenPAK chip. With this tool you can also read an already programmed chip and export its data to the Designer. Designer will generate a project, which has the same configuration as chip.

To start working with GreenPAK Designer please take the following steps:

- Download and install GreenPAK Designer software;
- Select what components you need;
- Interconnect and configure components;
- Specify the pinout;
- Test your design with the Emulation Tool (or Mini-Emulation tool for GreenPAK 2 chip);
- Use GreenPAK 1-4 development kit with GreenPAK 1-4 Programmer, GreenPAK 1-4 Emulation Tool, or GreenPAK 1 Mini-Emulation Tool to program your project into GreenPAK 1, GreenPAK 2, GreenPAK 3 and GreenPAK 4 chip. You can find your kit on Silego's webstore.

1.2 System requirements

PC System Configuration
Minimum System Requirements for Silego GreenPAK Designer:
CPU: 1800MHz
System Memory (RAM): 512MB
Graphics Card: 128MB
Free Hard Disk Space: 100MB
Operating System: Windows XP/Vista/7/8 (x86, x64), MAC OS X (v10.5) or Ubuntu 12.04

1.3 Support

Free support for GreenPAK Programmer is available online at http://www.silego.com.

At skype: silegousa
silegochinese
silegoeurope
silegojapan

At facebook: Silego-Technology

For software updates, please go to the Software & Docs page on our website.
You can find all these resources in the **Help** menu of GreenPAK Designer.

1.4 Acronyms

These are the acronyms used in the User Guide.

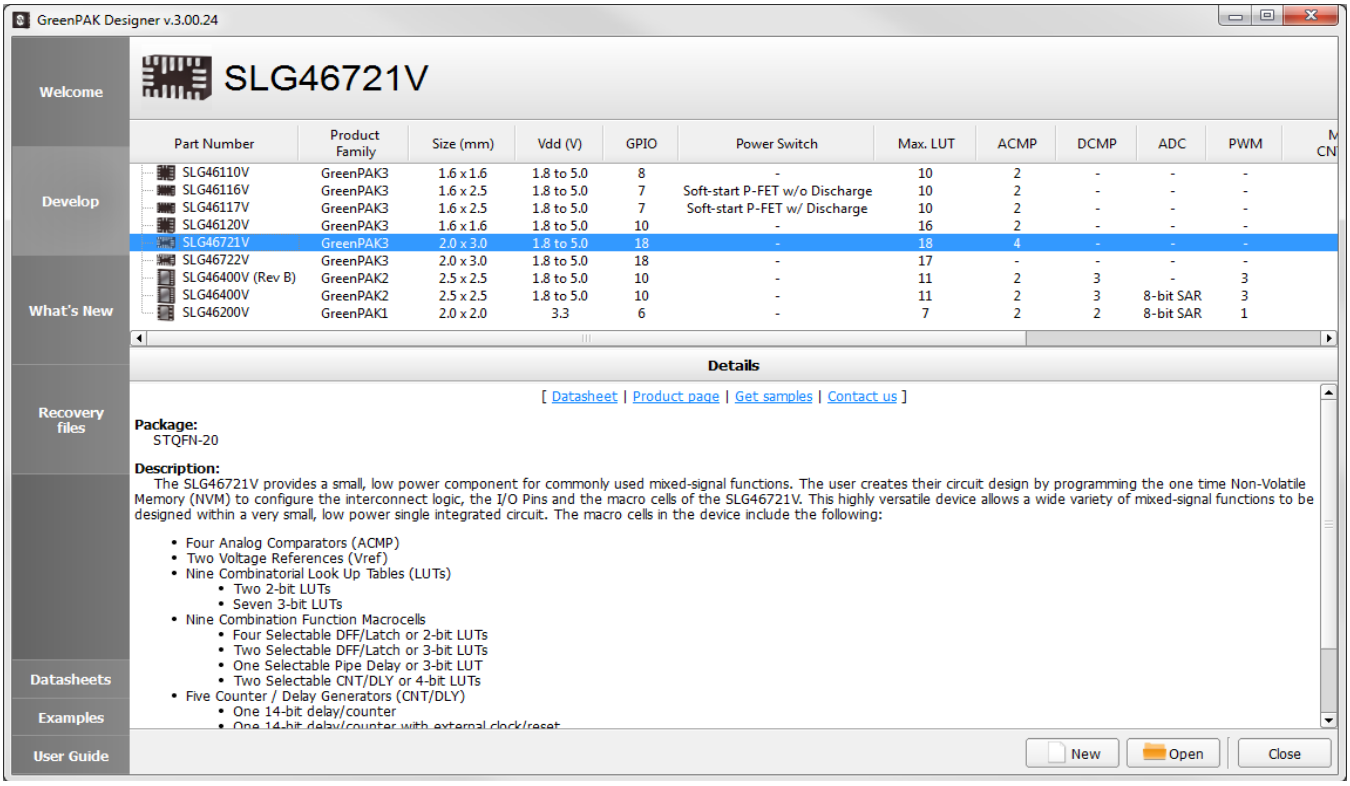
Table 1-1. Acronyms

Acronym	Description
GPD	GreenPAK Designer
GPP	GreenPAK Programmer
IDE	Integrated Development Environment
I/O	Input/Output
IC	Integrated Circuit
OE	Output Enable
USB	Universal Serial Bus
GPIO	General Purpose Input / Output
GPI	General Purpose Input
NMOS	N-channel MOSFET (metal-oxide-semiconductor field-effect transistor)
PMOS	P-channel MOSFET (metal-oxide-semiconductor field-effect transistor)

2. GreenPAK Designer Launcher

This section describes GreenPAK Designer launcher application and its features.

Figure 2-1. GreenPAK Designer Launcher User Interface


GreenPAK Designer v.3.00.24
Welcome
Develop
What's New
Recovery files
Datasheets
Examples
User Guide
SLG46721V
Part Number
Product Family
Size (mm)
Vdd (V)
GPIO
Power Switch
Max. LUT
ACMP
DCMP
ADC
PWM
SLG46110V GreenPAK3 1.6 x 1.6 1.8 to 5.0 8 - 10 2 - - -
SLG46116V GreenPAK3 1.6 x 2.5 1.8 to 5.0 7 Soft-start P-FET w/o Discharge 10 2 - - -
SLG46117V GreenPAK3 1.6 x 2.5 1.8 to 5.0 7 Soft-start P-FET w/ Discharge 10 2 - - -
SLG46120V GreenPAK3 1.6 x 1.6 1.8 to 5.0 10 - 16 2 - - -
SLG46721V GreenPAK3 2.0 x 3.0 1.8 to 5.0 18 - 18 4 - - -
SLG46722V GreenPAK3 2.0 x 3.0 1.8 to 5.0 18 - 17 - - - -
SLG46400V (Rev B) GreenPAK2 2.5 x 2.5 1.8 to 5.0 10 - 11 2 3 - 3
SLG46400V GreenPAK2 2.5 x 2.5 1.8 to 5.0 10 - 11 2 3 8-bit SAR 3
SLG46200V GreenPAK1 2.0 x 2.0 3.3 6 - 7 2 2 8-bit SAR 1
Details
[Datasheet | Product page | Get samples | Contact us]
Package:
STQFN-20
Description:
The SLG46721V provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macro cells of the SLG46721V. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macro cells in the device include the following:
Four Analog Comparators (ACMP)
Two Voltage References (Vref)
Nine Combinatorial Look Up Tables (LUTs)
Two 2-bit LUTs
Seven 3-bit LUTs
Nine Combination Function Macrocells
Four Selectable DFF/Latch or 2-bit LUTs
Two Selectable DFF/Latch or 3-bit LUTs
One Selectable Pipe Delay or 3-bit LUT
Two Selectable CNT/DLY or 4-bit LUTs
Five Counter / Delay Generators (CNT/DLY)
One 14-bit delay/counter
New
Open
Close

GreenPAK Designer launcher:

- Welcome – welcome page with short information and tips for new users.
- Develop – on this page user can select chip revision to start new project for required revision: SLG46200, SLG46400, SLG46400 Rev B, SLG46721, SLG46722, SLG46110, SLG46120, SLG46116, SLG46117, SLG46620.
- What's New – page with information about current projects and chips application.
- Recovery Files – page with restored files after crash or freeze. Files was saved with Autosave feature in predetermined time intervals.

New Project – starts new project for selected chip revision (or double-click with left mouse button on selected chip revision icon);
Open Project – opens existing project, automatically selects chip revision;
Close – close GreenPAK Designer launcher.

3. GreenPAK Designer

This section describes GreenPAK Designer application and its features.

3.1 GreenPAK Designer Interface Overview

GreenPAK Designer consists of: main menu, toolbar, main work area, output window, properties panel and components list (see Figure 3-1, Figure 3-2, Figure 3-3).

Figure 3-1. GreenPAK 1 User Interface

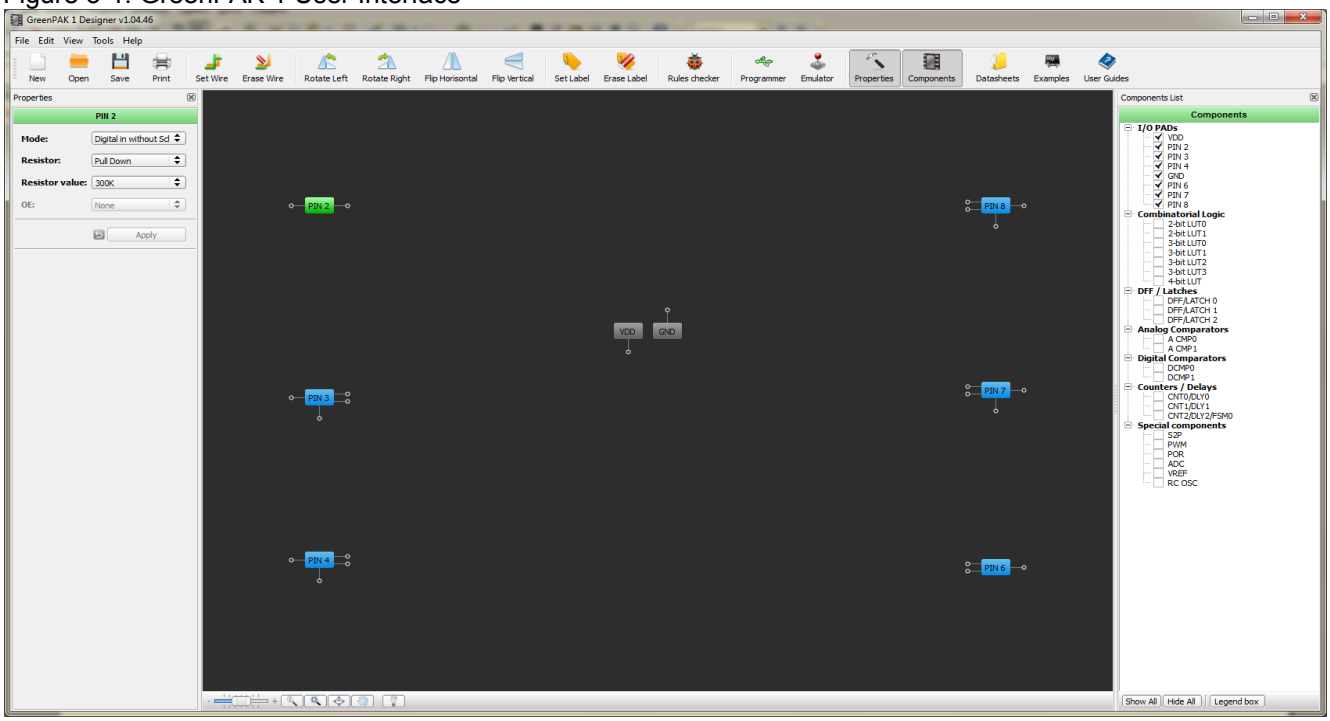


Figure 3-2. GreenPAK 2-3 User Interface

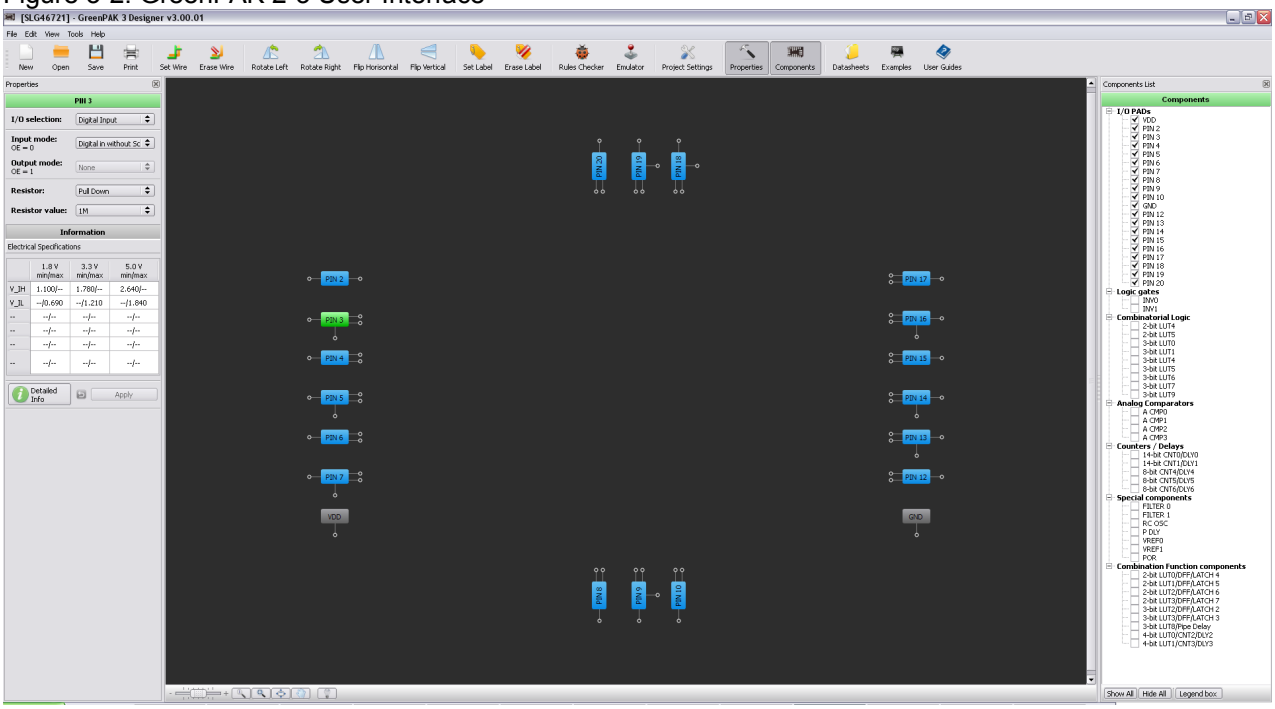
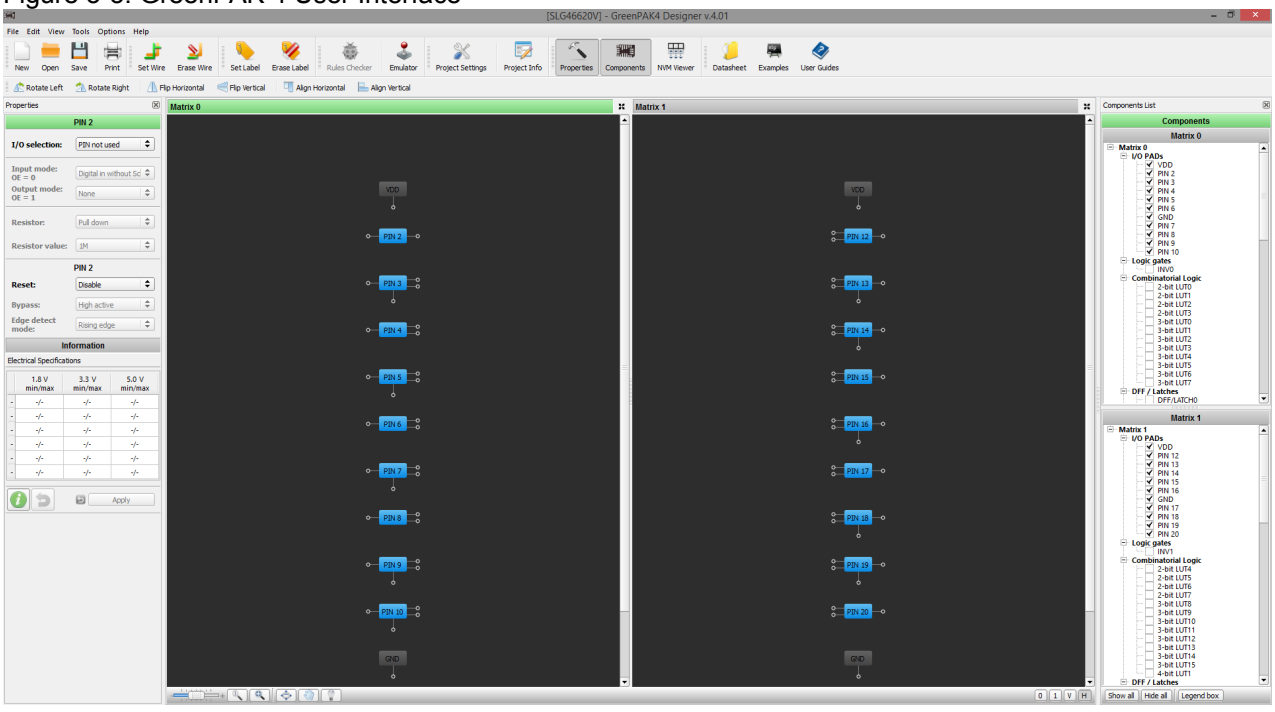


Figure 3-3. GreenPAK 4 User Interface



3.1.1. Main Menu

Main menu contains controls described below:

- **File**
  - New – start new or open existing project from GPAK Launcher;
  - Open – open existing project in GP Designer;
  - Clear – clear project and select revision for specified chip;
  - Open in current – open existing project for specified chip;
  - Save – save current project;
  - Save as – save current project in specified location;
  - Import NVM bits – load configuration bits from text file;
  - Export NVM bits – save configuration bits to text file;
  - Print – start Print Editor referring item 4;
  - Project Information;
  - Examples – open examples directory;
  - Exit program – close GPD;
- **Edit**
  - Rotate Left – rotate a selected block counterclockwise;
  - Rotate Right – rotate a selected block clockwise;
  - Flip Horizontal – horizontal reflection of a selected block
  - Flip Vertical – vertical reflection of a selected block
  - Align Horizontal – horizontal alignment of selected blocks
  - Align Vertical – vertical alignment of selected blocks
  - Set Label – creating a text label for selected blocks
  - Erase Label – erasing text labels near selected blocks
  - Set Wire – enable wire creating mode;
  - Erase Wire – enable wire erase mode;
- **View**
  - Zoom in – increase the work area scale;
  - Zoom out – decrease the work area scale;
  - Fit work area – tune scale to show all blocks visible in project;
  - Zoom 1:1 – set default scale;
  - Pan mode – enable;
  - Full-screen mode – switch to full-screen mode
  - Properties – show/hide Properties panel;
  - NVM Viewer – show/hide NVM bits viewer;
  - Components – show/hide Green PAK blocks list;
  - Rules Checker Output;
- **Tools (in GreenPAK 1 Designer)**
  - Emulation – this tool is included for convenient project testing;
  - Programmer – start GreenPAK Programmer with the current project exported;
  - Rules Checker – checks current design for correct settings;

- **Tools (in GreenPAK 2 Designer)**
  - Emulator – this tool is included for convenient project testing;
  - Mini-Emulator – this tool is included for convenient project testing;
  - Rules Checker – checks current design for correct settings;
- **Tools (in GreenPAK 3-4 Designer)**
  - Emulator – this tool is included for convenient project testing;
  - Rules Checker – checks current design for correct settings;
- **Options**
  - Settings – default projects folder, autosave, toolbars position, recovery, shortcuts and update options;
- **Help**
  - Help – show help window
  - User guide – open User guide directory;
  - Legend box – show the legend box in the right bottom;
  - Silego web site – open Silego official web site;
  - Software and documentation – open Software & Dock web page;
  - Support page – FAQ web page;
  - Facebook – Silego technology Facebook page;
  - Silego TV – Silego technology YouTube channel;
  - Examples – open examples directory;
  - Datasheets – open documentation directory;
  - Updater – open GreenPAK product page;
  - About this program – show information about GPD versions modification.

3.1.2. Tool-bars

Toolbar provides a quick access to frequently used functions. There are 7 tool-bars:

- **File**
  - New;
  - Open;
  - Save;
  - Print;
- **Wire**
  - Set wire;
  - Erase Wire;
- **Item editor**
  - Rotate Left;
  - Rotate Right;
  - Flip Horizontal;
  - Flip Vertical;
  - Align Horizontal;
  - Align Vertical;

- Set Label;
- Erase Label;

- **Tools (in GreenPAK 1 Designer)**
  - Rules Checker;
  - Programmer;
  - Emulator;
- **Tools (in GreenPAK 2 Designer)**
  - Rules Checker;
  - Mini-Emulator;
  - Emulator;
  - Lock NVM;
- **Tools (in GreenPAK 3-4 Designer)**
  - Rules Checker;
  - Emulator;
  - Project Settings;
  - Project Info;
- **Panel switcher**
  - Properties;
  - Components;
  - NVM Viewer;
- **Help**
  - Datasheets;
  - Examples;
  - User Guides;
- **Navigation**
  - Zoom slider – adjust scale;
  - Zoom 1:1;
  - Fit work area;
  - Full screen mode;
  - Pan mode;
  - Show item hint;

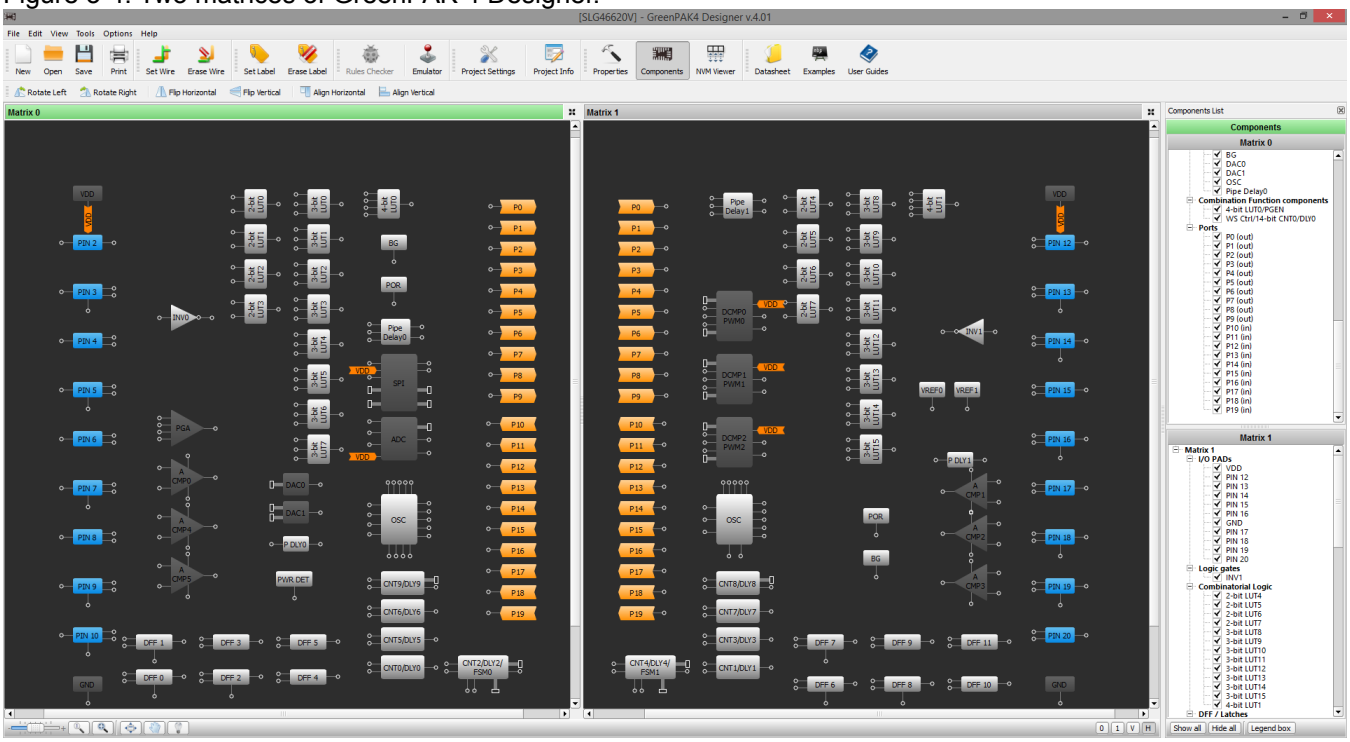
3.1.3. Work Area

Work area contains all blocks available in GreenPAK chip and their connections. In GreenPAK 4 Designer (SLG46620 chip) work area consist of 2 matrices: Matrix0 and Matrix1(Figure 3-4). The components of each matrix can be interconnected through 10 input and 10 output ports.

Matrices window placement define buttons:

- Matrix 0 (full screen);
- Matrix 1 (full screen);
- Vertical placement (2 matrices);
- Horizontal placement (2 matrices);
- One of matrices in separate window or monitor.

Figure 3-4. Two matrices of GreenPAK 4 Designer.



Three types of components connection:

- Connectivity matrix connections (green) – user can connect any output to any input through wiring tool;
- Settings defined connections (orange) – these connections are predefined and depend on block settings;
- Buses (wide orange line) – buses also depend on block settings. All buses are 8-bit wide.

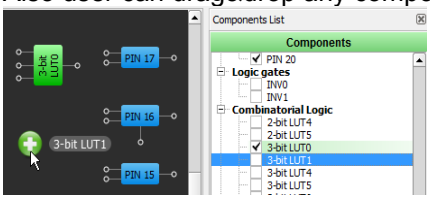
All blocks can be moved using mouse or keyboard (Ctrl+Arrow Keys or Alt+Arrow Keys) and rotated. You can move a few blocks at the same time by using multiple select option. Rotation, flipping and alignment is also available for more than one block at a time.

3.1.4. Properties Panel

Properties panel contains all settings available for selected chip component. The panel is divided in two partitions: **Properties** and **Connections**. Properties division contains settings and parameters that could be specified for a selected block. Connection division contains settings which control the predefined connections to the selected block. Last division could not be present in some blocks. Some parameters and settings are common for a few blocks. There are 2 types of controlling elements **Edit Box** and **Drop List.** To change settings in Drop List you can click and select action or place the mouse pointer over selected list and scroll by mouse wheel. To enter value into the Edit Box you can use keyboard, mouse scroll or buttons at the right. After finishing all configurations press **Apply** button to confirm changes. If you want to discard changes you can press **Reset** button left from the **Apply** button or select another block.

3.1.5. Components List

The Components list is an instrument that contains all blocks available in chip. It provides user with the possibility to show/hide unused blocks. You cannot hide blocks that are connected by any type of lines. In the GreenPAK chip there are connections which are beyond the connectivity matrix. They are controlled by settings of proper components and cannot be fully disconnected. That's why there are some blocks that cannot be hidden. Hidden blocks retain their configuration. For this reason, be sure to configure hidden components properly. You can show/hide selected blocks by using the check/un-check feature on the list. In order to show a group of blocks, double-click on the check box of the desired group. In order to hide a group use a single click.
There are two buttons at the bottom of the components list – Show all (shows all blocks) and Hide all (hides all blocks which are not connected to a circuit). Also user can use filter to find required components.
Also user can drag&drop any component from Component List to the workarea to the right place:



3.1.6 Color Scheme

Components:

Mode		Description
Normal	Selected	
		Turned on
		Turned off
		I/O PAD

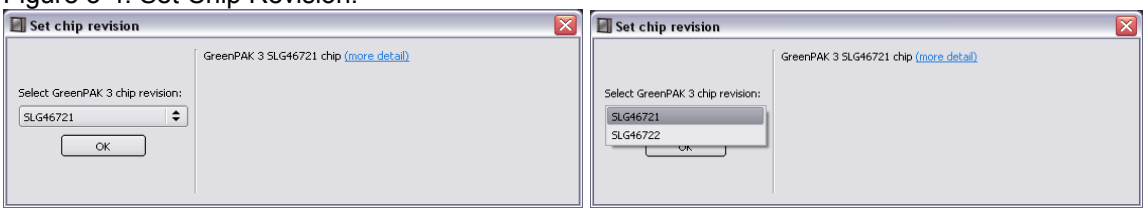
Components Pin Tips:

Color	Value
	User can connect wire to this pin
	Pin has already been connected (and there cannot be any other connections to this pin)
	User can connect wire to this pin only after changing component option
	Inner connection, user cannot connect wire to this pin
	External I/O Pin (I/O from chip)

3.2 Creating a Project

To create a new GreenPAK Designer project go to **File->New** or click the "New" icon on the toolbar. While creating new project in GreenPAK 2-3 Designer please choose chip revision for current project.

Figure 3-4. Set Chip Revision.



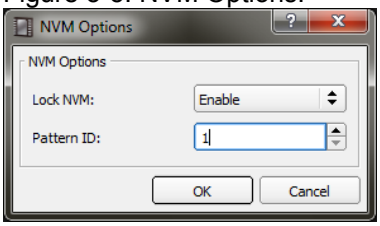
A new project will be created in current window and all unsaved changes will be lost. Also you can start a new GreenPAK Designer copy and it will be loaded with the blank project. By default the project is configured for minimal power consumption and some components are disabled. All disabled components are darker and colored in red after selection. GreenPAK 1 project uses [.gpp/gp1] file extension, GreenPAK 2-4 projects use [.gp2,.gp3,.gp4] file extension. It contains information about position, rotation/flipping and configuration of chip blocks, all wire connections, and bit file sequence settings of test mode, etc. Interface settings will not be saved in the Project file.

3.2.1 Updating Existing Projects

If you load an existing project created by a previous version of GreenPAK Designer and want to save changes, it will be saved in the updated file format.

3.2.2 Lock NVM Window

Figure 3-5. NVM Options.

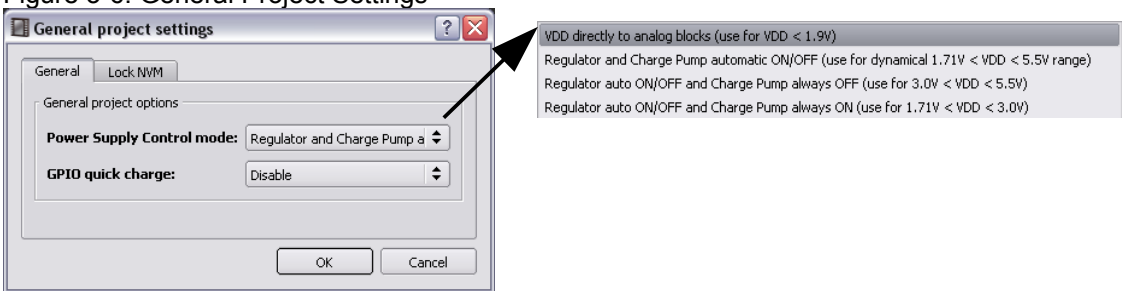


Lock NVM – blocks NVM reading. A programmed project becomes unavailable for chip reading. Though chip is still applicable for the emulation.

Pattern ID – gives an ID (1-255) to the project. The ID will be put in the chip after programming, and also will be read back during "chip reading" operation.

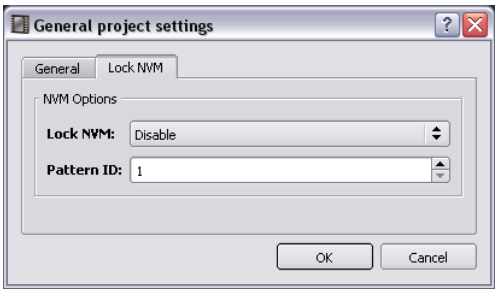
3.2.3 Project Settings Window

Figure 3-6. General Project Settings


General project settings
General
Lock NVM
General project options
Power Supply Control mode:
Regulator and Charge Pump a
GPIO quick charge:
Disable
OK
Cancel
VDD directly to analog blocks (use for VDD < 1.9V)
Regulator and Charge Pump automatic ON/OFF (use for dynamical 1.71V < VDD < 5.5V range)
Regulator auto ON/OFF and Charge Pump always OFF (use for 3.0V < VDD < 5.5V)
Regulator auto ON/OFF and Charge Pump always ON (use for 1.71V < VDD < 3.0V)

GPIO quick charge – this option will temporarily enable 2k resistor for ~1µs duration in parallel to internal pull-up/downs during power on, before reset signal is released to internal blocks. For example, this option should be used to ensure the internal pull-up rise-time is fast enough to be detected as high level during power-on. Otherwise, a rising edge with weak internal pull-up can be quite slow, and miss detection as a high-level because of too slow of risetime.

Figure 3-7. Project Settings

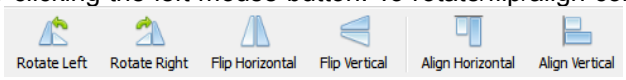


Lock NVM – blocks NVM reading. A programmed project becomes unavailable for chip reading. The chip is still applicable for emulation.

Pattern ID – gives an ID (1-255) to the project. The ID will be put in the chip after programming, and also will be read while “chip reading” operates.

3.3 Configuring Chip Components

3.3.1 Placing Components

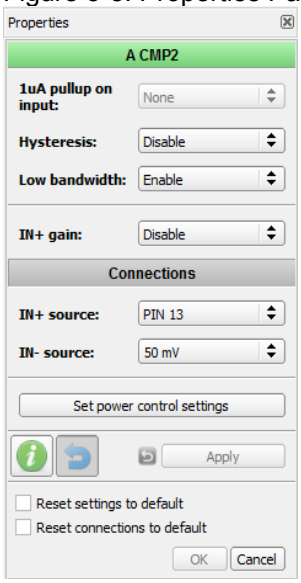
When you open GreenPAK Designer it will start with a blank project. A blank project contains pins and blocks which cannot be hidden. Components can be moved, rotated, flipped and aligned. In order to move a component, simply drag it where you want by clicking the left mouse button. To rotate/flip/align component select it and press the "Rotate/Flip/Align" buttons 

on the toolbar or select Rotate/Flip/Align in the main menu.

3.3.2 Setting Chip Components Parameters

Each chip component has different parameters. Some components have parameters that are shared with other components. Changes in one block cause changes in other blocks. Component settings are available at component **Properties** panel (Figure 3-8) which appears after double-clicking on the component. **Properties** panel consists of three parts: Properties, Connections, and Information. Properties section contains all settings of a selected component. Connections section allows you to configure connections that couldn't be made using wiring tool. Information section contains short information about parameters of selected component. After making changes in **Properties** panel click the **"Apply"** button to save changes. If you do not click the **"Apply"** button and select another block, a save changes message box will appear.

Figure 3-8. Properties Panel



Reset connections and/or settings to default: this option allows to reset NVM bits, components properties, wire connections from/to component.

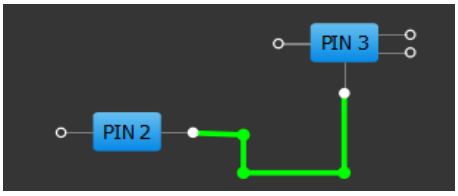
3.4 Specifying Interconnections

You can interconnect chip components to achieve the necessary functionality. To make a connection please select **Set wire** on the **Wire** toolbar or from the main menu. Next, click the first and second pins that you want to connect. After selecting the first pin, GPD highlights allowed connections in green. If you click the first pin and then decide to exit line creating mode press **Esc** or the right mouse button.

Figure 3-9.

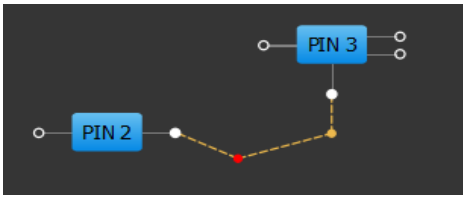
Also you can manually correct the created wires.
You can move horizontal lines up and down, vertical lines left and right (Figure 3-10).

Figure 3-10.



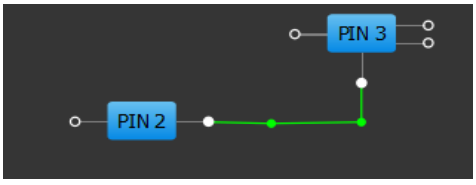
You can move points on the wire (Figure 3-11).

Figure 3-11.



In order to create additional points on the line use the double click (Figure 3-12).

Figure 3-12.



Only the green color pins can be connected Using Wire Creating tool. Some components have pins that are not allowed to be connected using wiring tool. Connections between such pins (orange dotted line and violet pin color) and buses can be made only by changing settings in **Connections** section of the **Properties** panel of

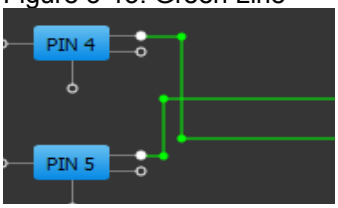
proper components. In this case violet pins can change color to green and user can connect them using wiring tool. Orange wires will be automatically generated. Orange wires also can be modified by user. Input pins without connections are considered to be tied to ground.

In order to delete wire please select **Erase wire**

at the **Wire** tool-bar and click on the selected wire. Only green wires can be deleted.

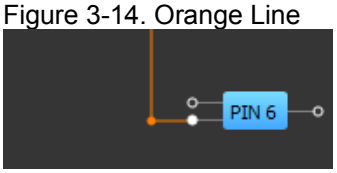
3.4.1 Wire Types

Figure 3-13. Green Line



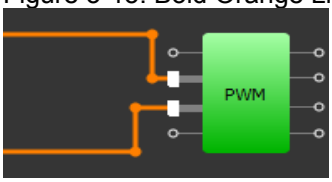
Green lines in GreenPAK Designer software tools are used to mark manual wires. Using them you can manually connect necessary blocks to operate in the desired way. You can connect block output to multiple inputs, but wiring of different outputs to one input is impossible.

Figure 3-14. Orange Line



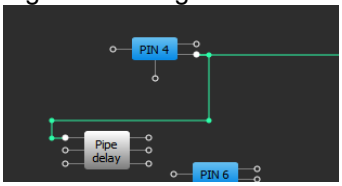
Orange lines are used to mark the internal functional bounds of the chip blocks. They do not have the impact on chip operation until the proper function is used. These lines can't be erased.

Figure 3-15. Bold Orange Line



Bold orange lines (like the orange lines) mark the internal bounds. The difference is that the bold orange lines mark 8-bit parallel data buses. These lines also cannot be erased. They do not have an impact on chip operation until the proper function is used and the proper option is set.

Figure 3-16. Light Green Line

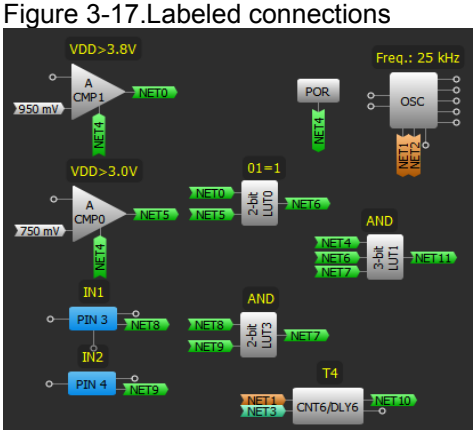


Light green lines are used to mark the shared connections. Their behavior is the same as the green lines.

Replacing wires by labels

This option converts wired connection to 2 labels (for output and input pins) and back (Figure 3-17). Name of the label will be generated automatically: NETx, where x – random number. If output was connected to few inputs all of them should have the same name. For changing the connection type use the context menu of the block, line or label(NET).

Figure 3-17.Labeled connections



Available options for wire (context menu):

- Convert to labeled connection;

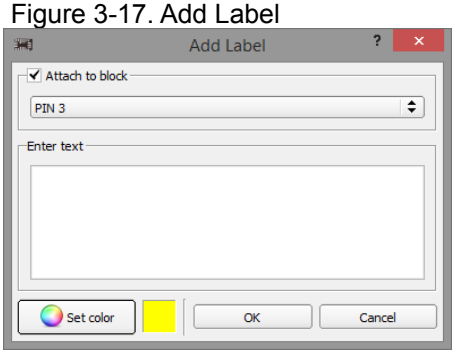
Available options for label (context menu):

- Convert to wired connection;
- Rename network;
- Remove connection.

3.4.2 Set/Erase Label

Using Set/Erase Label the user can add/delete text label. The Set Label tool adds a text label to the selected component or without connecting them to the specific component. The user can Attach label to component or Detach label(s) from component(s). If no component is selected, then the user can select a component from the list offered by the Set Label tool. The user can also choose text color. If the selected component already has a label, Set Label tool can edit label text. If the user selects more than one component, it is possible to change the text color without changing text in all components at once. If the user changes the text while more than one component is selected, it will be changed on all selected components at once as well. Erase Label deletes text label.

Figure 3-17. Add Label



3.5 Specifying the Pinout

3.5.1 Port Connections

Pin blocks can be connected just like any other blocks using the Wiring Tool.

3.5.2 Port Drive Modes

GreenPAK 1 chip has five PGIO (PIN3,4,6,7,8) and one GPI (PIN2) pin components. These components can be configured to work in the following modes:

- Digital in with Schmitt trigger;
- Digital in without Schmitt trigger;
- Low voltage digital in;
- Analog I/O;
- 1x push pull;
- 2x push pull;
- 1x open drain;
- 2x open drain;

GreenPAK 2 chip has nine PGIO (PIN3,4,5,6,8,9,10,11,12) and one GPI (PIN2) pin components. These components can be configured to work in the following modes:

- Digital in with Schmitt trigger;
- Digital in without Schmitt trigger;
- Low voltage digital in;
- Analog I/O;
- 1x push pull;
- 2x push pull;
- 1x open drain;
- 2x open drain;
- Analog in and open drain out;

GreenPAK 3-4 chip has seventeen PGIO (PIN3,4,5,6,7,8,9,10,12,13,14,15,16,17,18,19,20) and one GPI (PIN2) pin components. These components can be configured to work in the following modes:

- Digital in with Schmitt trigger;
- Digital in without Schmitt trigger;
- Low voltage digital in;
- 1x push pull;
- 2x push pull;
- 1x open drain NMOS;
- 2x open drain NMOS;
- 4x open drain NMOS;
- 1x open drain PMOS;
- 2x open drain PMOS;
- 1x 3-State Output
- 2x 3-State Output
- Analog input;
- Analog output;

Also, Pull-Up/Pull-Down resistors are configurable. To configure the pin component, open its parameters to set a desired mode and pull-up/pull-down resistor. I/O pin components have **input (IN)**, **output (OUT)** and **output**

enable (OE) pins. These pins are one-way directed, so you need to configure the pin component and connect the proper pin. OUT pin is an output signal from the pin component. It corresponds to the signal from the input buffer. IN pin is an input to the pin component. It accepts a signal from internal components. Output Enable (OE) signal defines the Push-pull buffer state. Low OE signal switches buffer to Hi-Z state. High OE signal enables Push-pull buffer regardless of selected component operating mode. It could be used for applications where bidirectional pins are needed.

3.6 Navigation

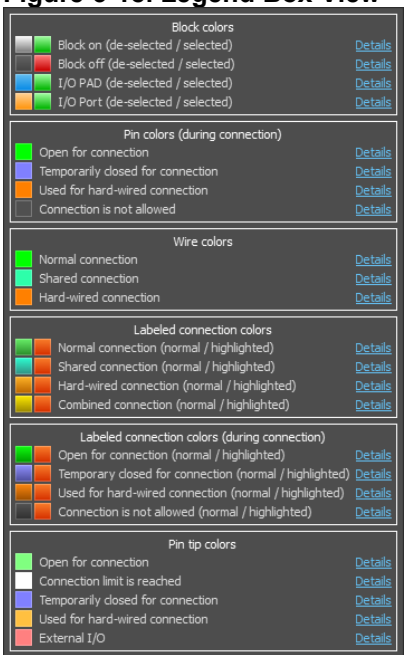
To navigate through project workspace use the **View** menu or toolbar. Use **Zoom In**, **Zoom Out** buttons or slider to zoom workspace. If you want to see all project components click on **Fit work area** or **Zoom 1:1**. To navigate through work area you can use **Pan mode**.

To enable block's hint, press **Show item hints** button. A hint box pops up next to the item when the mouse moves over the block.

3.7 Legend Box

Legend box shows the color scheme of GreenPAK designer. After clicking 'Details', this box displays. The user can open this window by clicking 'Legend box' button in 'Help' menu.

Figure 3-18. Legend Box View

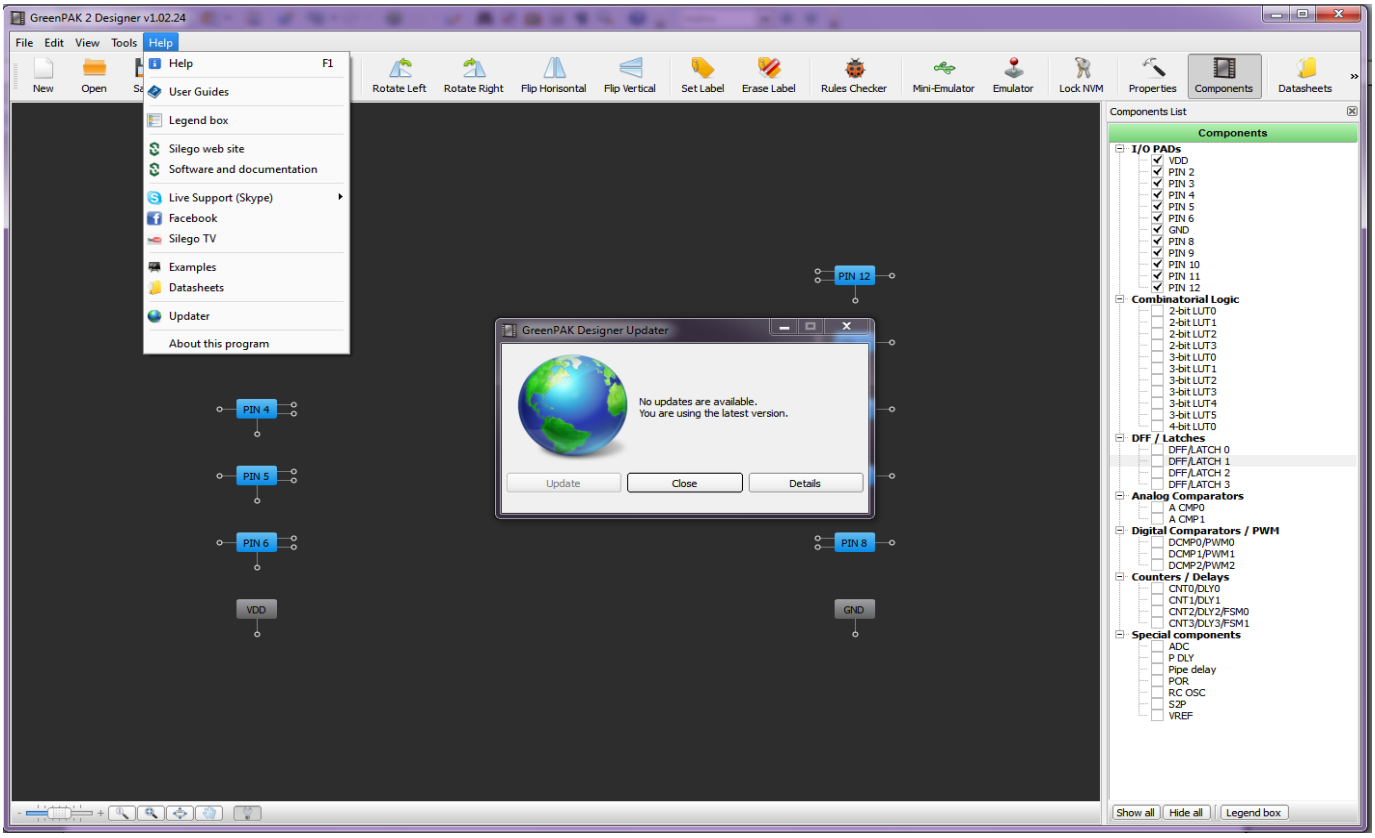

Block colors
Block on (de-selected / selected) Details
Block off (de-selected / selected) Details
I/O PAD (de-selected / selected) Details
I/O Port (de-selected / selected) Details
Pin colors (during connection)
Open for connection Details
Temporarily closed for connection Details
Used for hard-wired connection Details
Connection is not allowed Details
Wire colors
Normal connection Details
Shared connection Details
Hard-wired connection Details
Labeled connection colors
Normal connection (normal / highlighted) Details
Shared connection (normal / highlighted) Details
Hard-wired connection (normal / highlighted) Details
Combined connection (normal / highlighted) Details
Labeled connection colors (during connection)
Open for connection (normal / highlighted) Details
Temporary closed for connection (normal / highlighted) Details
Used for hard-wired connection (normal / highlighted) Details
Connection is not allowed (normal / highlighted) Details
Pin tip colors
Open for connection Details
Connection limit is reached Details
Temporarily closed for connection Details
Used for hard-wired connection Details
External I/O Details

3.8. Updating GreenPAK Designer

There are two ways of updating the GreenPAK Designer.

1. When updates are available – this information will be displayed. The user will get a chance to either download a new version using the “Update” , or the “Not now” to delay the renewal until the next program start. After the download is finished, an opened folder with installer will appear.

Figure 3-19. Updating GreenPAK Designer

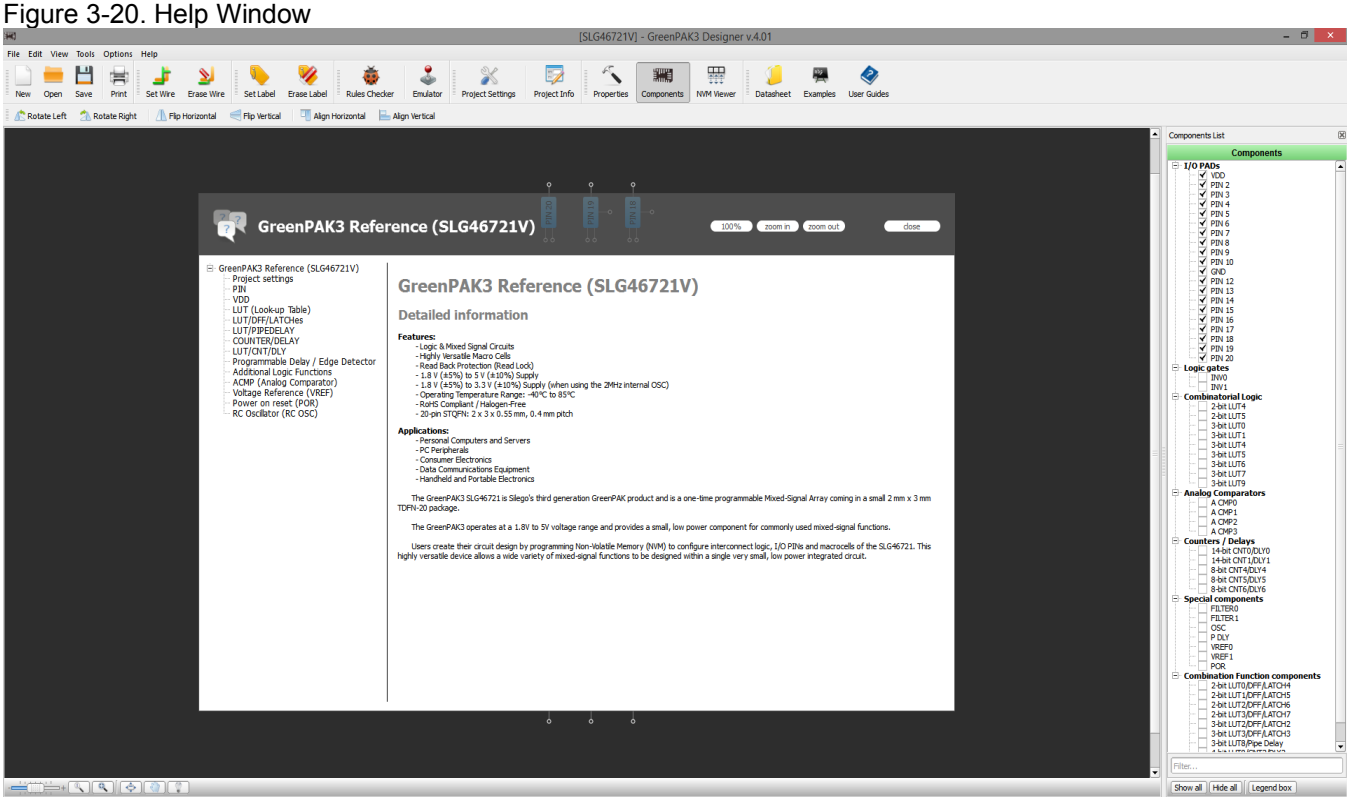


2. You can also find the latest GPD version at Software & Docs page of Silego web site. For the best user experience, keep your GreenPAK Designer up to date. Feel free to email suggested updates to the developer to improve this program (Please refer to **“About this program”** section of **Help** menu).

3.9 Help Window

To view information about a specific block, select the block and click 'Help' from the Help menu or press the 'F1' button. A window will list the information about each block ('short info'). Press the 'detailed info' button for more detailed information (Figure 3-20). If you don't select any block, you will be shown the information about all the blocks. The 'Help' button on the property panel of each block provides the same information about the current block.

Figure 3-20. Help Window

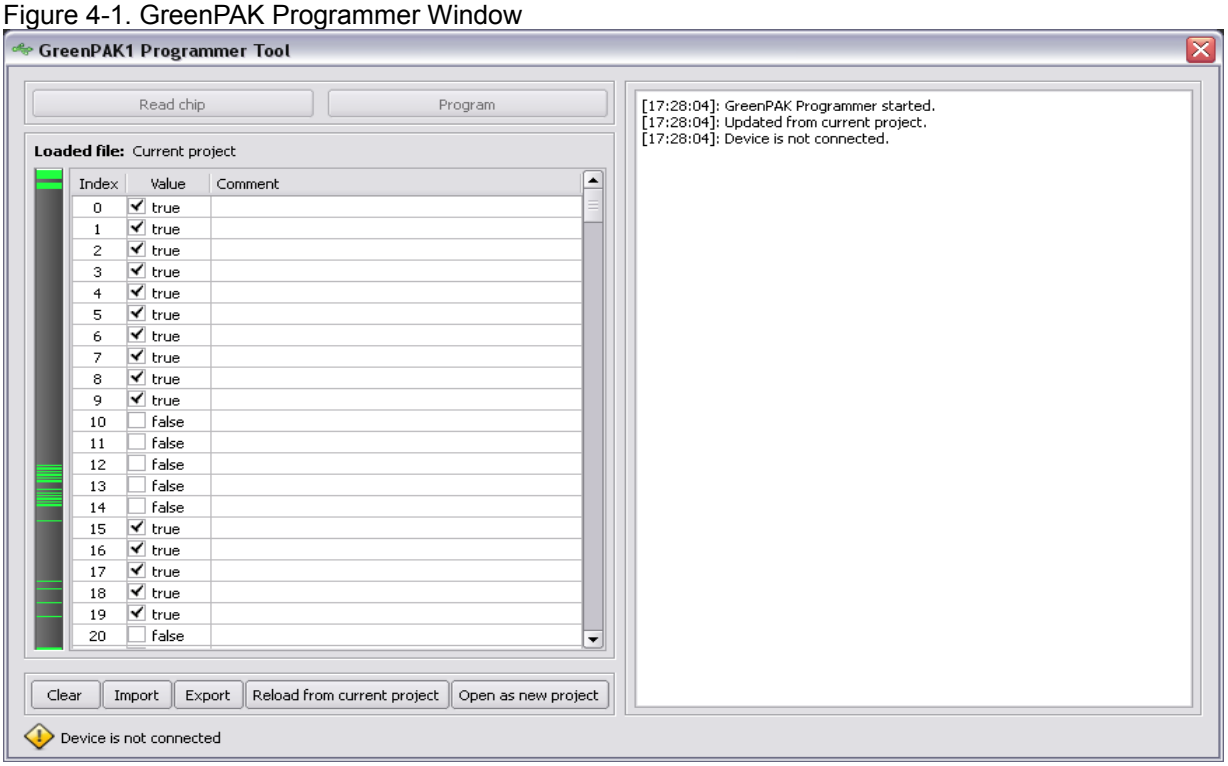


4. GreenPAK Programmer

4.1. GreenPAK Programmer Overview

GreenPAK Programmer provides user with a possibility to program a configured design to PAK chip quickly. It can be started from Designer software or from the Windows main menu. To start Programmer from GreenPAK Designer, use the Tool-bar main menu button or press **F10** on the keyboard. Programmer starts with an advanced interface shown on Figure 4-1.

Figure 4-1. GreenPAK Programmer Window



4.2. Selecting Sequence File

When you start GPP from the GPD tool-bar or the main menu, it automatically imports a bit sequence from the current project, so you can easily program the chip. Also, you can select another file sequence by pressing the **“Import”** button.

4.3. Programming Chip

To program da evice please follow the next steps:

- Insert PAK chip into the socket.
- Connect programmer hardware to USB. If you insert it for the first time please wait until programmer installation is complete. Next you will see the message, **“**Device is connected” in the status bar.
- Start GreenPAK Programmer
- Select file sequence if required.
- Press **Program** button.

- After programming is complete you will see a “Programming successful” message. If you see another message please refer to one of resources from the **Support** section.

4.4. Read Chip

For chip reading press the **Read chip** button. Alternatively, you can create a new file sequence manually.

4.5. Exporting Data to GPD

Using the GPP tool you can read an already programmed chip and export the data to GreenPAK Designer. Designer generates a project which has the same configuration as the chip. Components will be connected and configured but their placement will be the same as in a blank project. The exported project will be created in the new window. To export chip data to the GPD, press **Read chip** to read data and press **Open as new project** afterward.

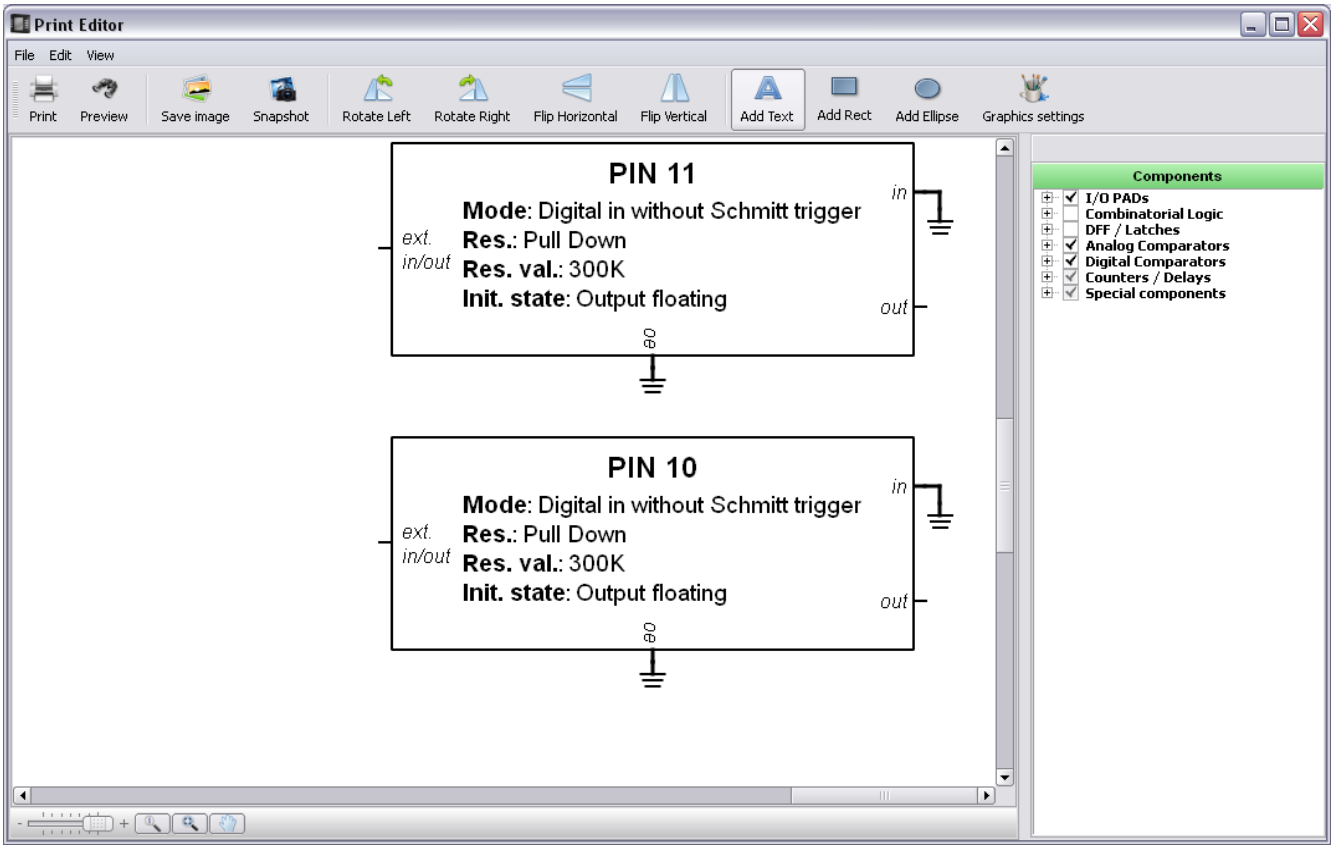
5. Print Function

Print Function component consists of two main parts:

- Editable working area, where the user can customize positions, view of components, and lines connecting them.
- Preview window where the user can set up the print preferences.

Editable working area shows all components which where used in the design.

Figure 5-1. Print Editor



The Main Actions:

- User can hide or display any component using the Components list on the right.
- Each component in the work area is selectable and movable.
- Any component can be rotated or flipped.

Note: print editor settings will be saved before print editor's window is closed. It allows the user to repair previous state during next opening.

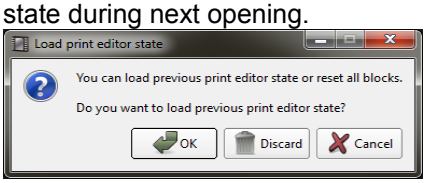

Load print editor state
You can load previous print editor state or reset all blocks.
Do you want to load previous print editor state?
OK
Discard
Cancel

Figure 5-2. Preview Window

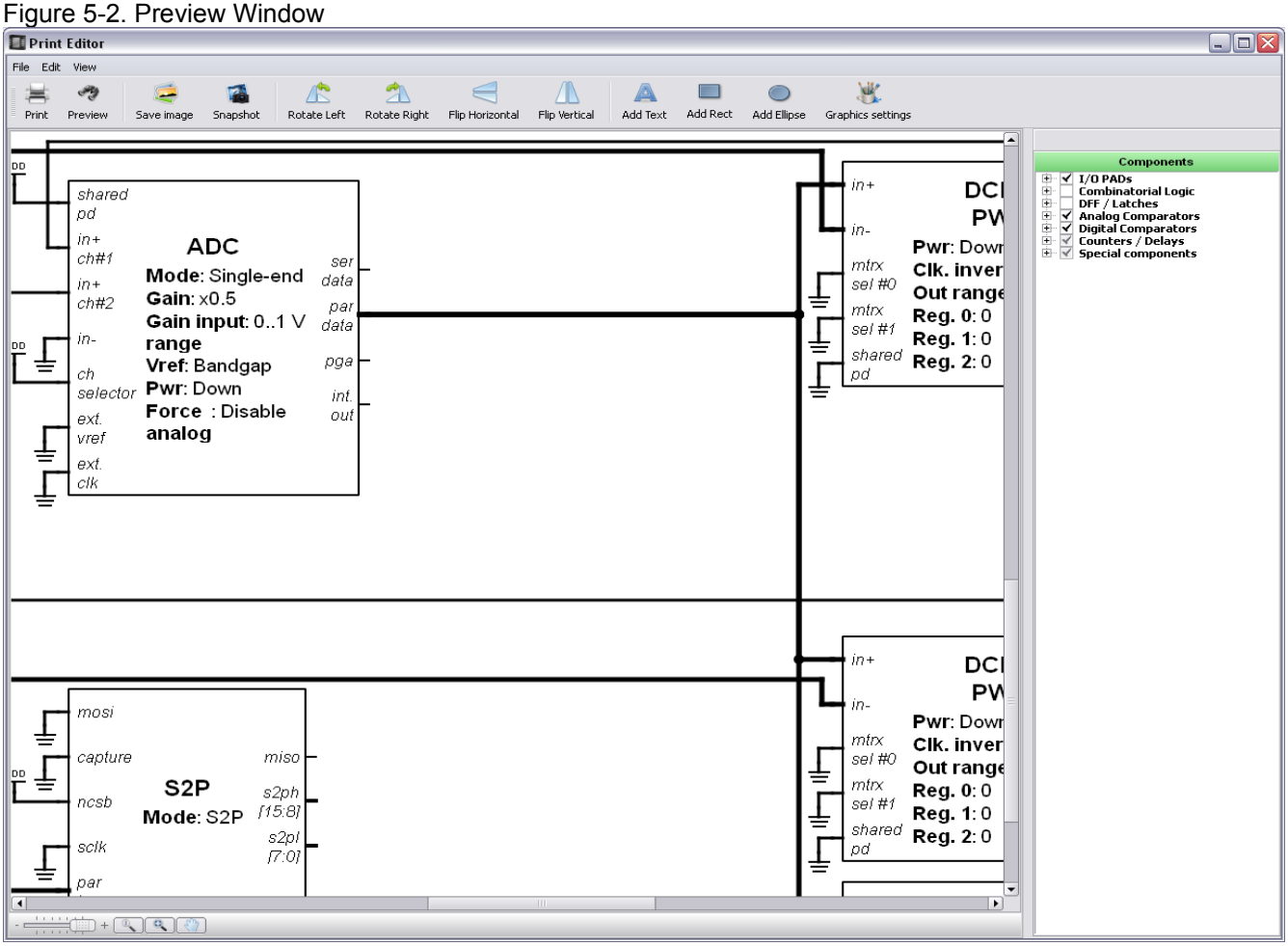
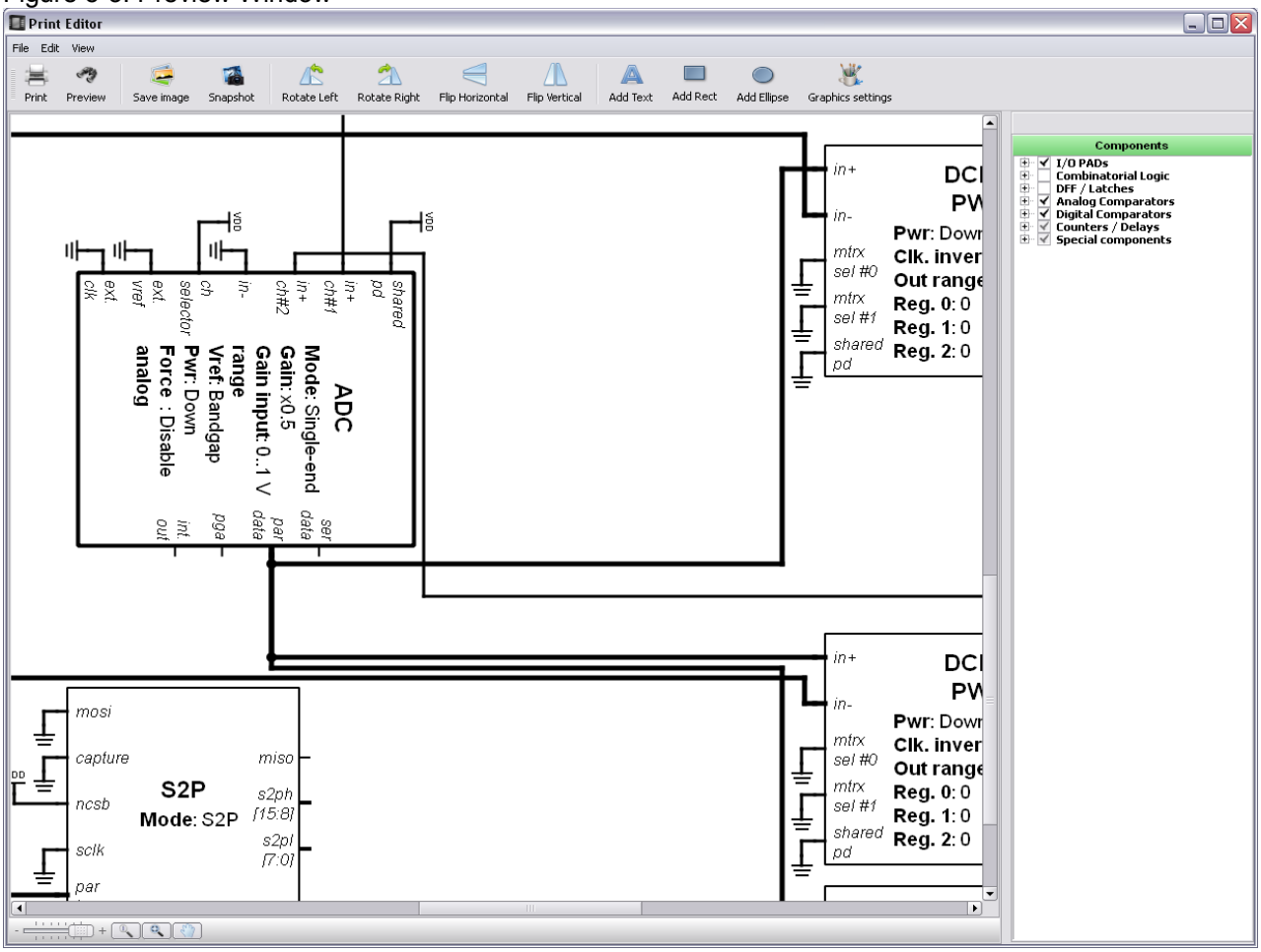
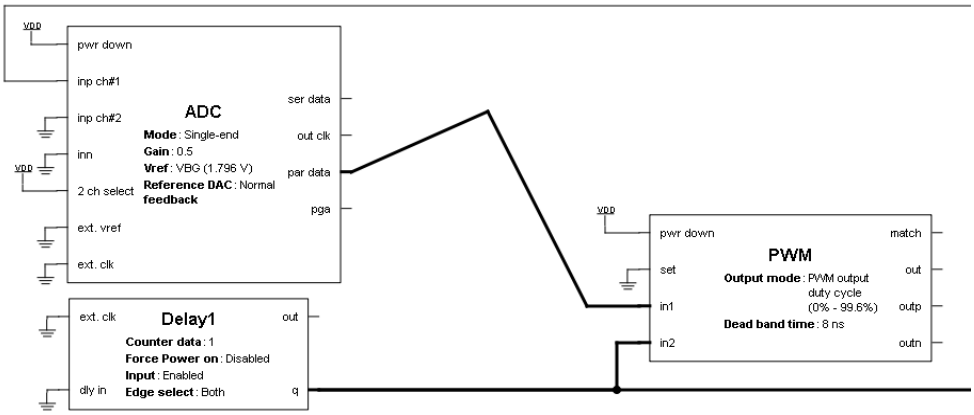


Figure 5-3. Preview Window



User can move lines and points to correct odd angled appearance.

Figure 5-4. Work sheet.



5.1. Working Area

Working area can be zoomed in or zoomed out.

User can add a text label to the schematics using the text tool.

Figure 5-5. Text Label

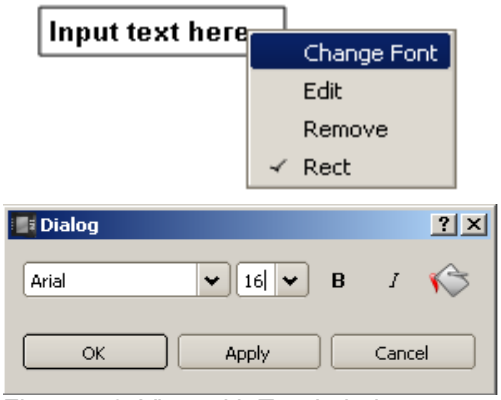
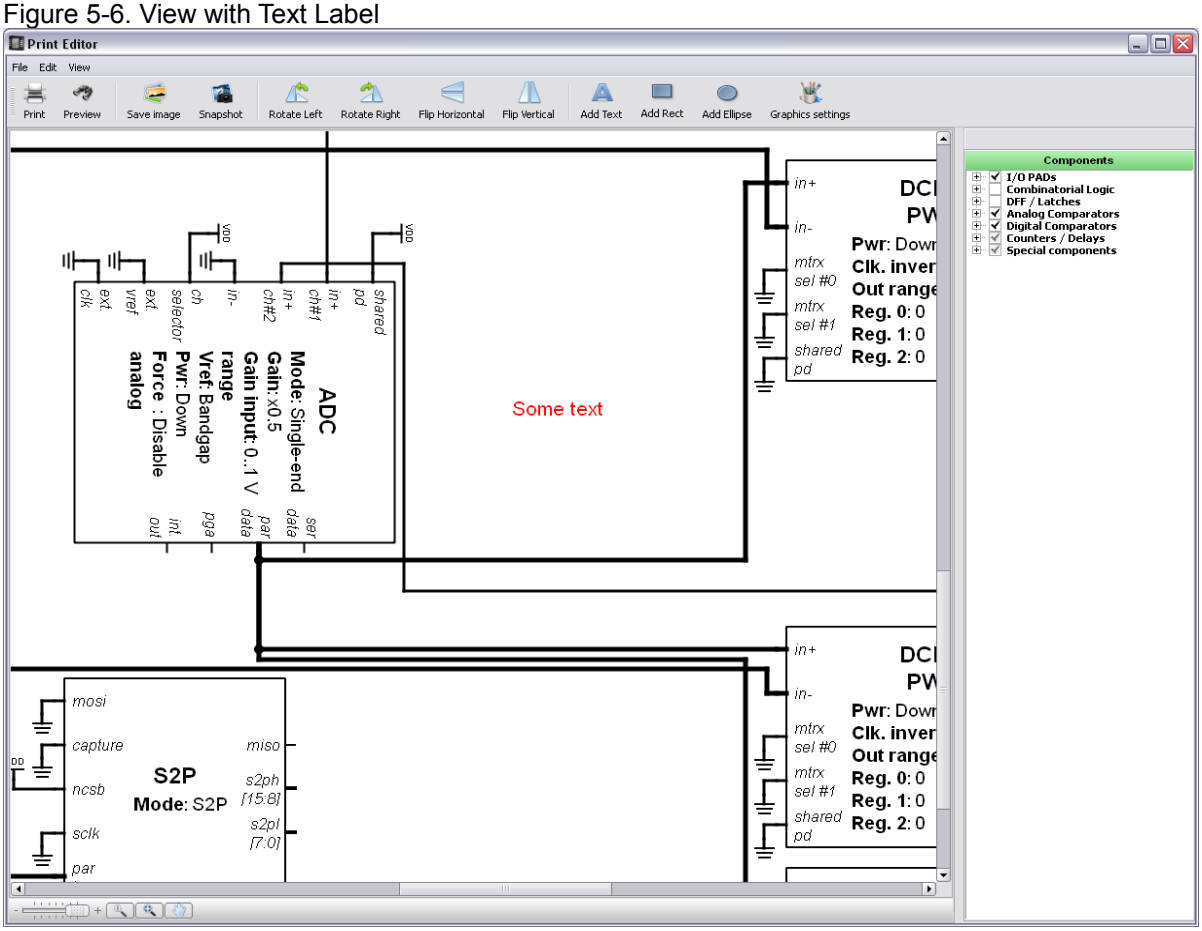
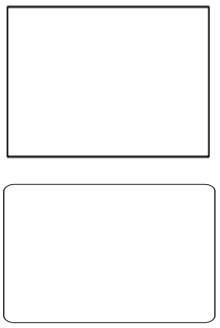


Figure 5-6. View with Text Label



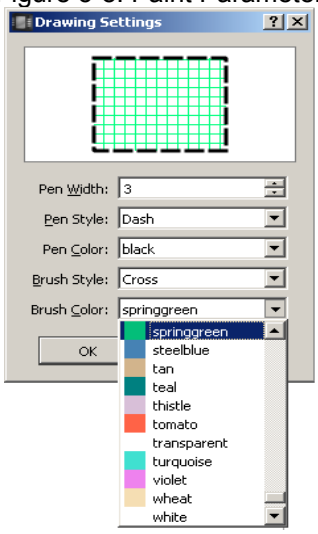
The user can add to the working area the custom figures including rectangle, rounded rectangle, ellipse etc.

Figure 5-7. Custom Figure



The user can also customize the main paint parameters.

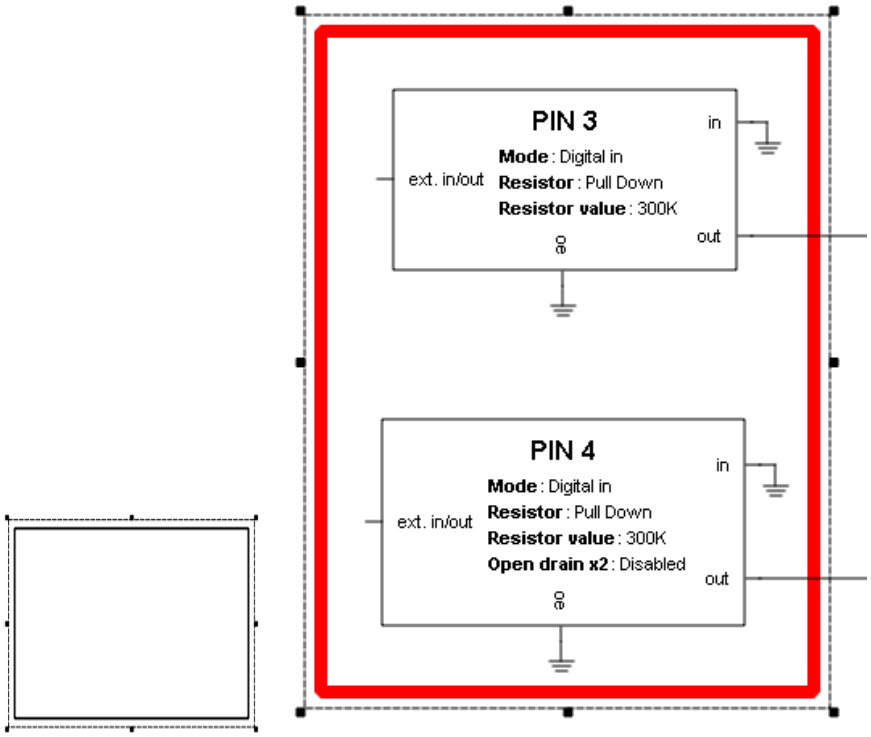
Figure 5-8. Paint Parameters



You can see a small preview window which includes a painted rectangle with user-parameters.

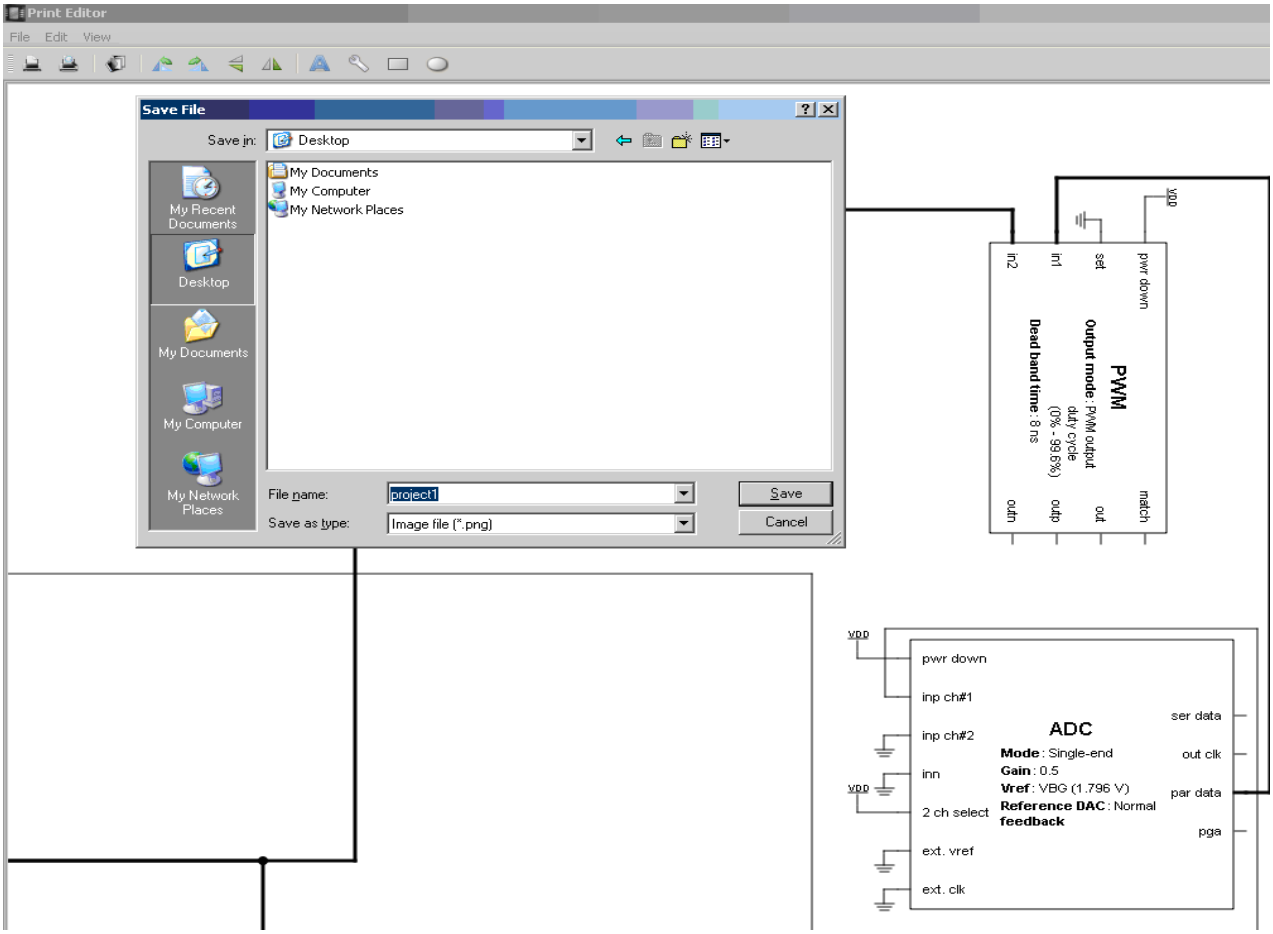
When the user adds a figure to the working area, one can customize the figure size by dragging black points on the corners and sides. The user can view it only by moving the mouse pointer up to the figure.

Figure 5-9. Work Area



The user can save a composed diagram into a graphics file or directly send it to the printer.

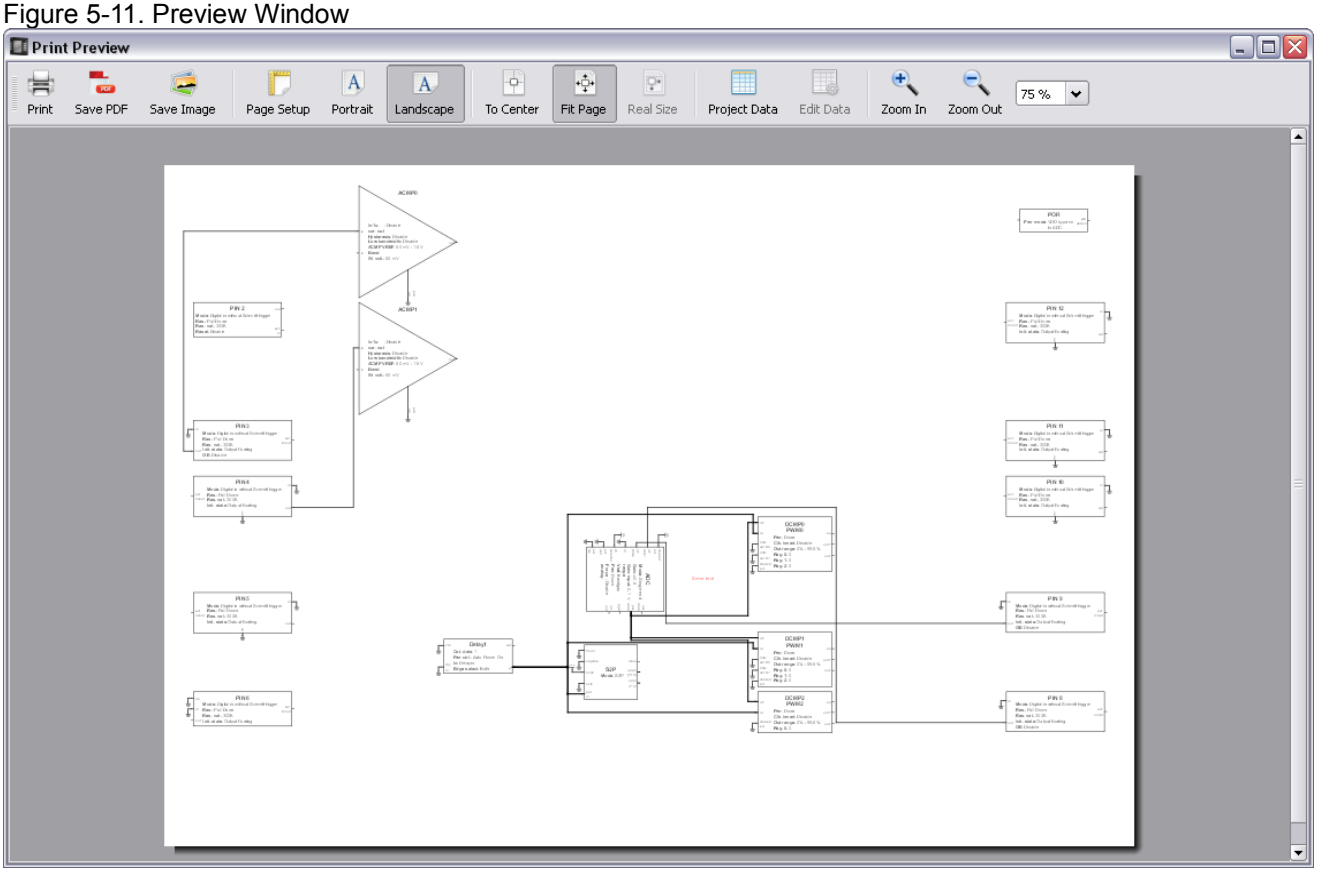
Figure 5-10. Save diagram



5.2. Preview Window

Preview window shows the composed and ready-to-print diagram. In this window, the user cannot change the position of the components or the other elements in the diagram. The user can only choose the advanced settings for printing or saving to the file.

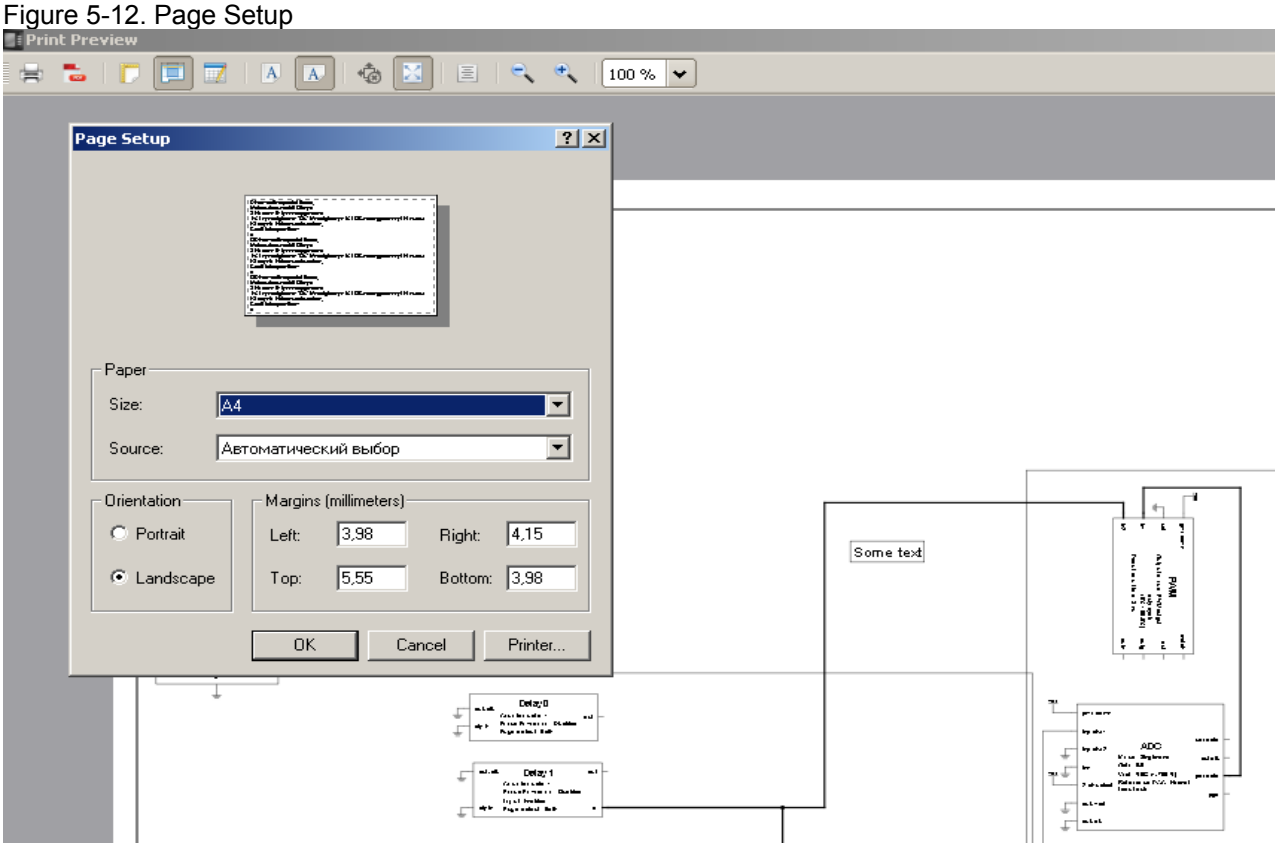
Figure 5-11. Preview Window



Main Actions
The user can:

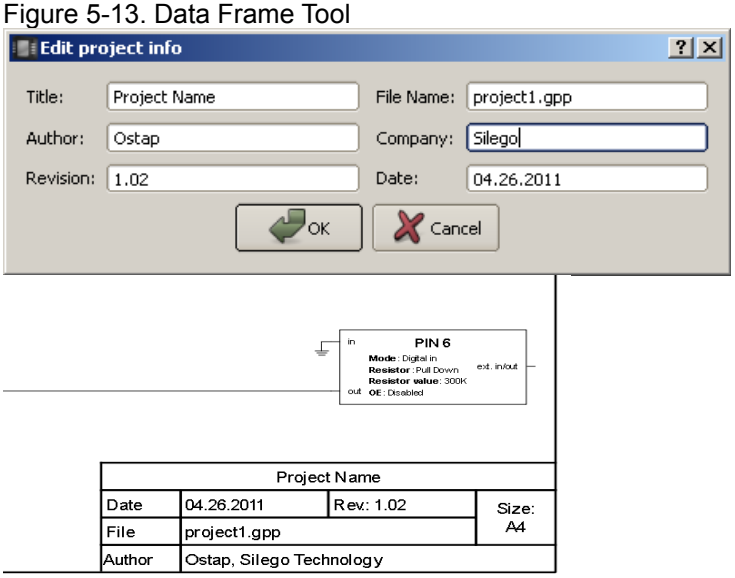
- Choose orientation of the diagram on a paper (landscape or portrait)
- Fit the diagram to a page or keep the real size
- Fit to center
- Zoom in or zoom out
- Choose the size or type of paper

Figure 5-12. Page Setup



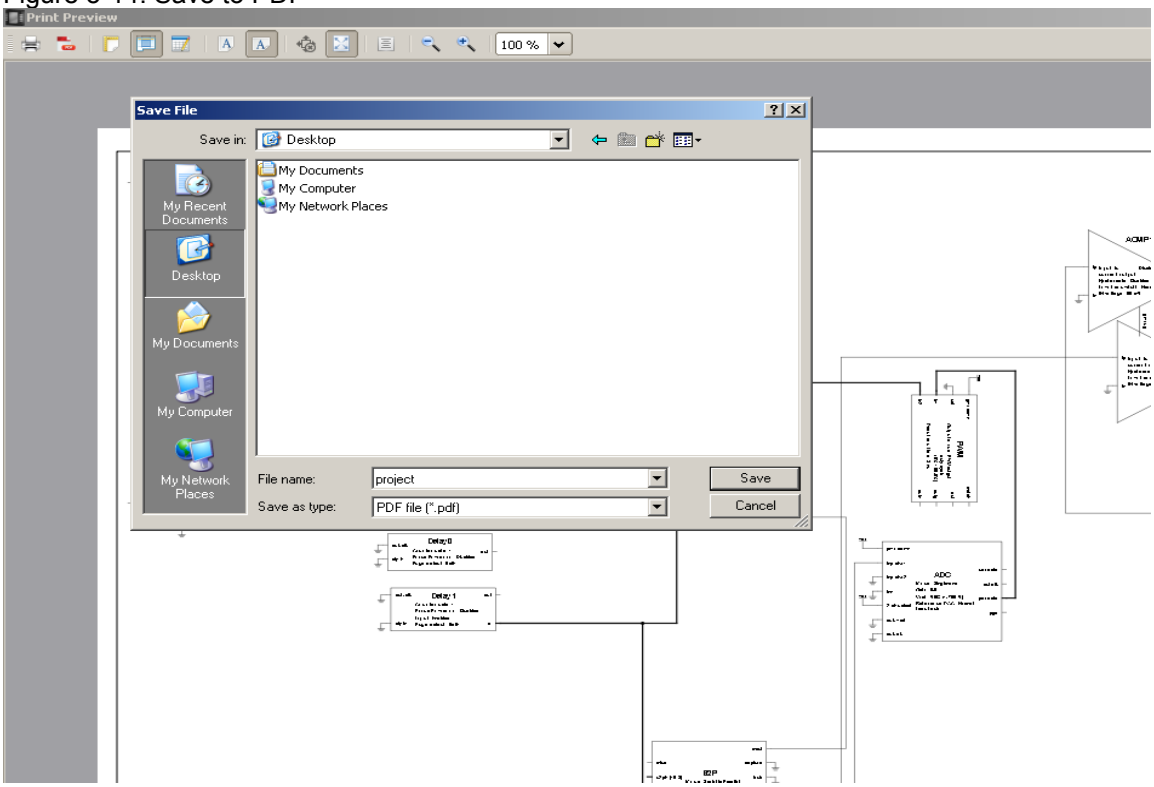
The user can add an editable data frame using the data frame tool.

Figure 5-13. Data Frame Tool



The user can save the finished diagram into a PDF file or print it out.

Figure 5-14. Save to PDF



6. Rules Checker

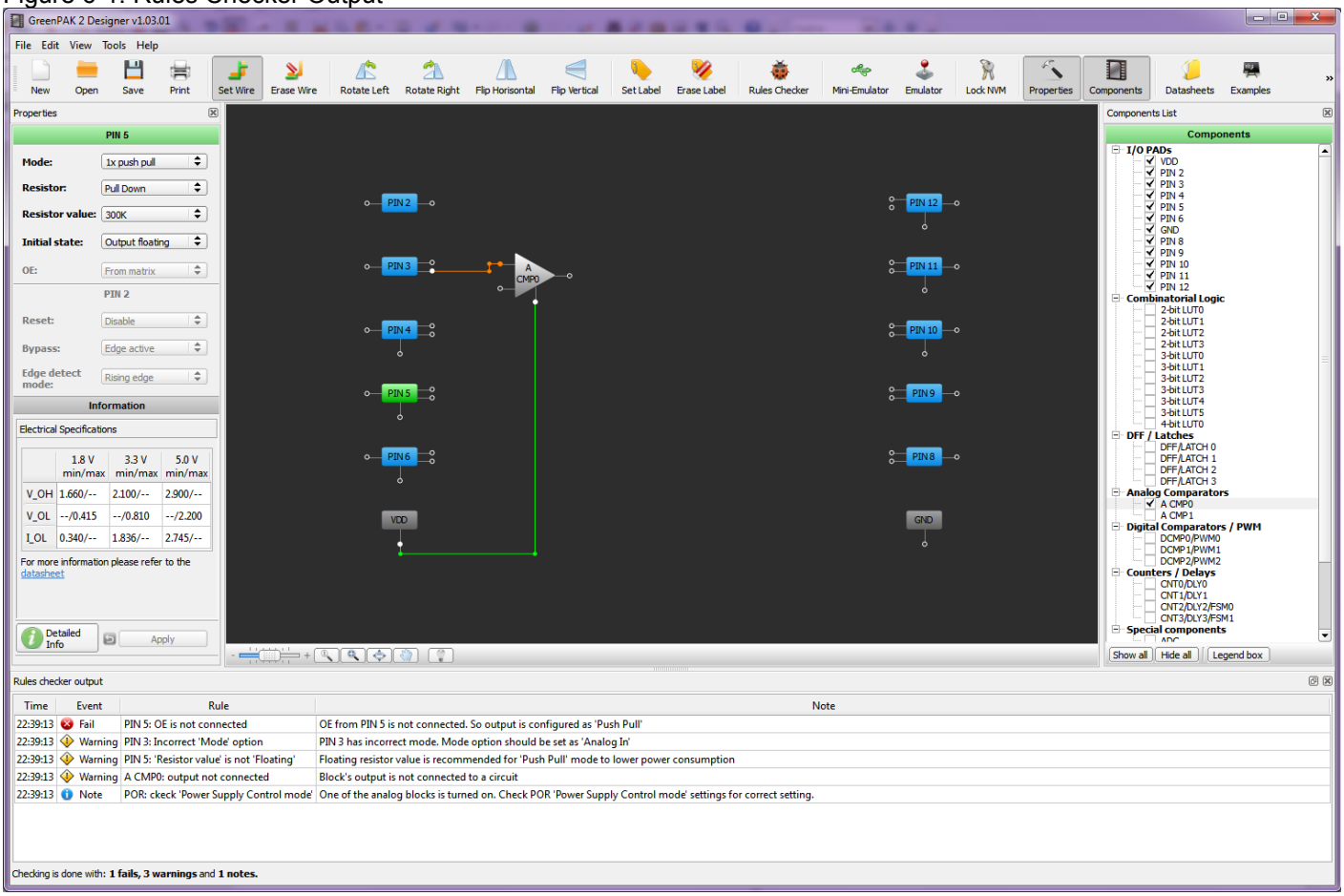
This tool allows checking current project errors, for example, incorrect block connections or settings. Rules Checker has three types of messages:

Fail - this message is generated when there is a significant error in design that will not work under any conditions.

Warning - this message is generated when one or more blocks may contain incorrect connections or settings in the design. This does not mean that there is an error. It only notifies the user to check the connections or settings of the blocks.

Note - this message is generated to remind the user to check for correct settings.

Figure 6-1. Rules Checker Output



In order to check the design, click the Rules Checker button on the tool bar in Tools menu.
Rules Checker Window can be called by clicking Rules checker output in View menu.
Rules checker output consists of three parts:

1. Event – shows message type (Fail, Warning, Note).
2. Rule – information about the message.
3. Note – recommendations on how to correct the error, or error explanation.

7. GreenPAK 1 Emulation Board

Figure 7-1. The Main Screen

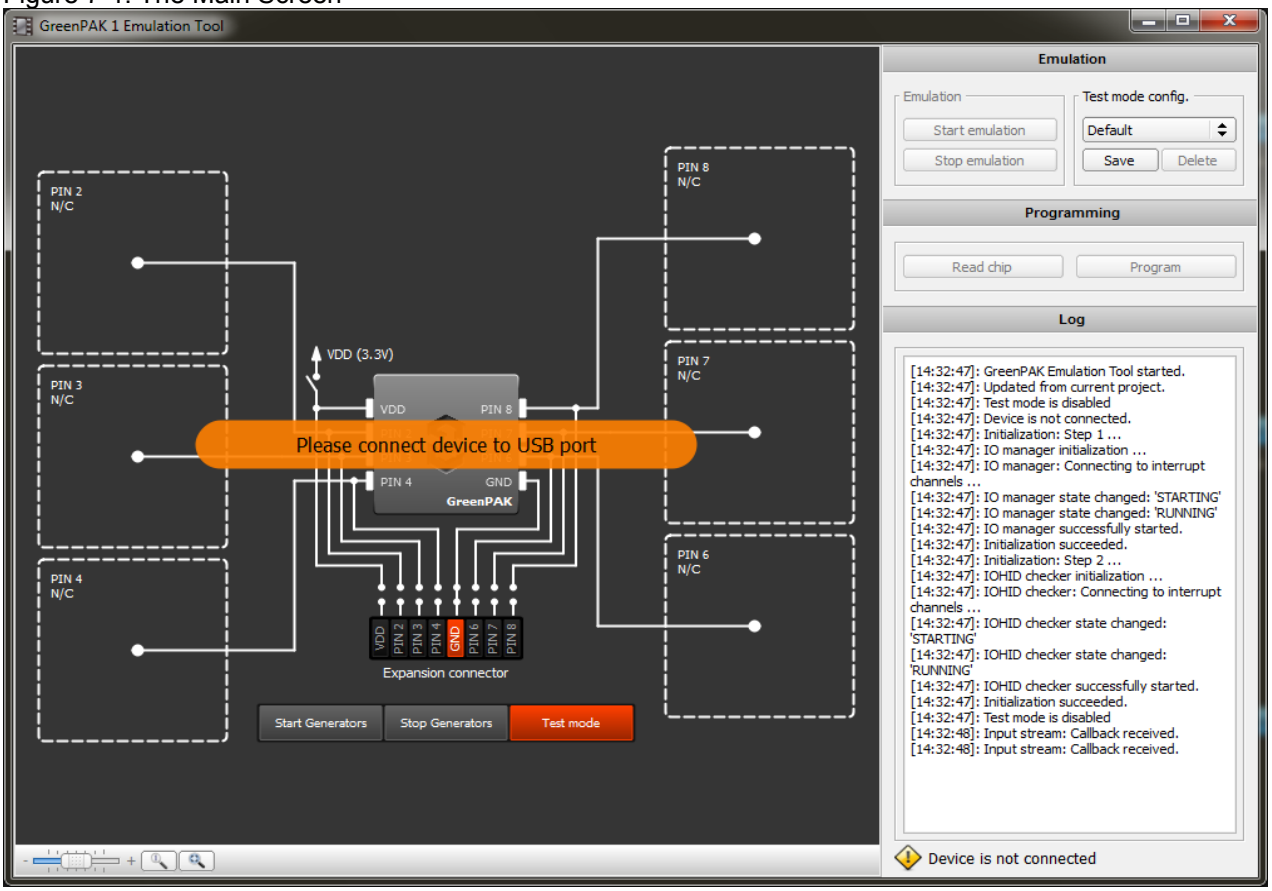
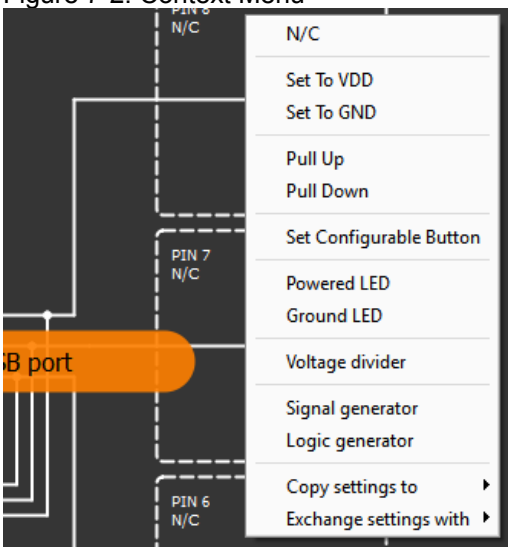


Figure 7-1 displays the GreenPAK IC with 6 dotted areas and expansion connectors which are connected to pins.

Dotted areas are used to configure input connections. Use the context menu to manage them.

Figure 7-2. Context Menu



7.1. Types of Areas

Non-Configurable Inputs (Figure 7-3 – 7-9):

Figure 7-3. N/C (not connected)

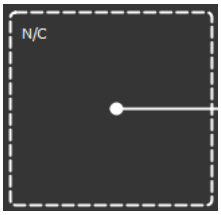


Figure 7-4. Set to VDD

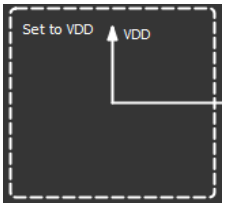


Figure 7-5. Set to GND

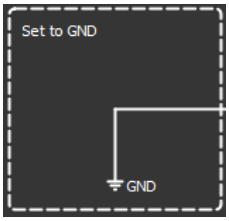


Figure 7-6. Pull Up

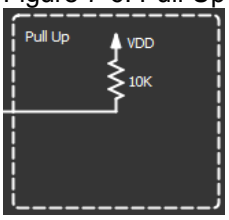


Figure 7-7. Pull Down

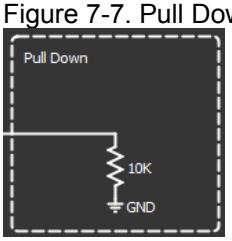


Figure 7-8. PWR LED

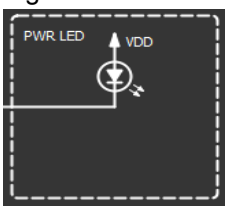
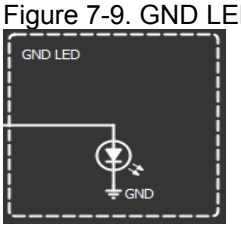
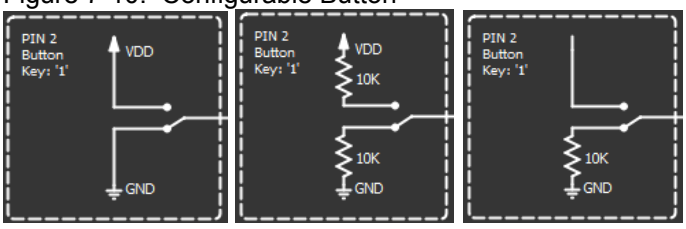


Figure 7-9. GND LED



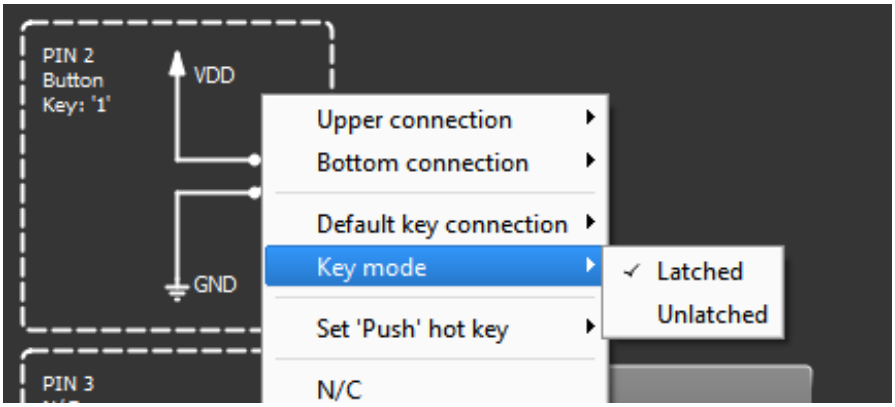
Configurable Inputs:

Figure 7-10. Configurable Button



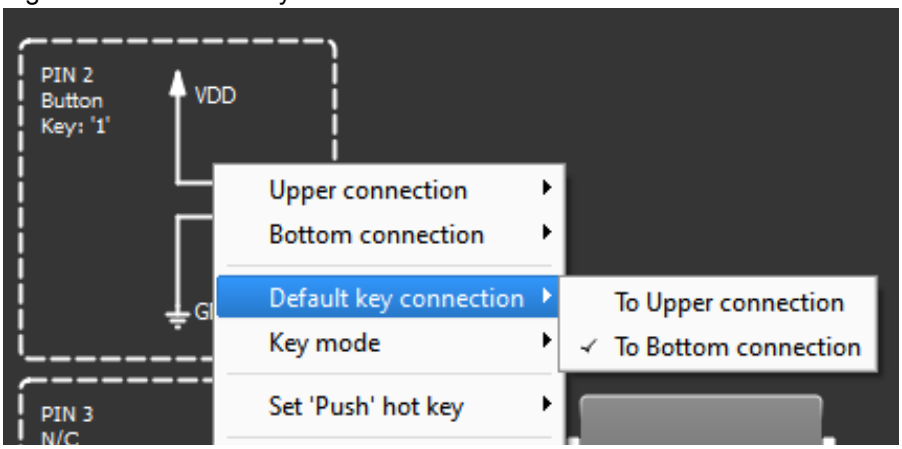
In the above mode you can switch between VDD and GND. Click your mouse over the key to change the value. The switch has 2 modes: Latched, Unlatched (default), which can be configured from the context menu:

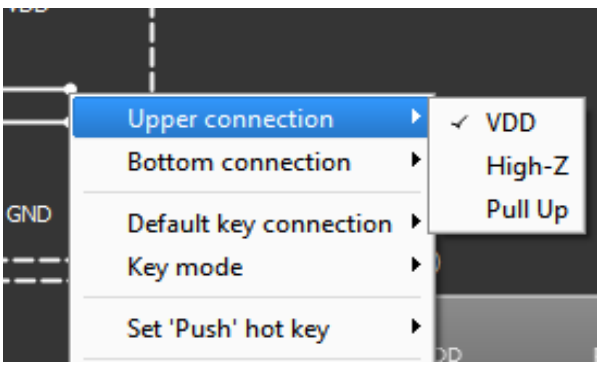
Figure 7-11. Key Mode

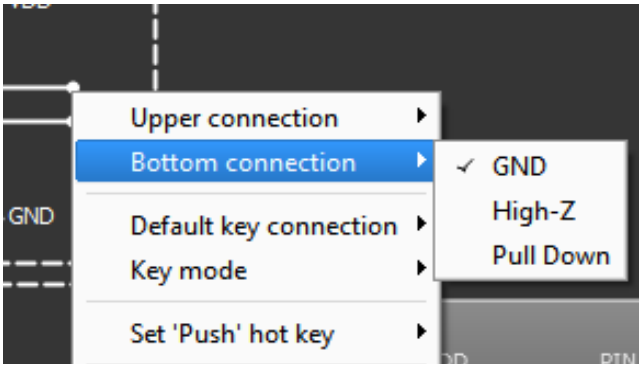


The default connection can be set to either Upper connection or Bottom connection.

Figure 7-12. Default Key Connection





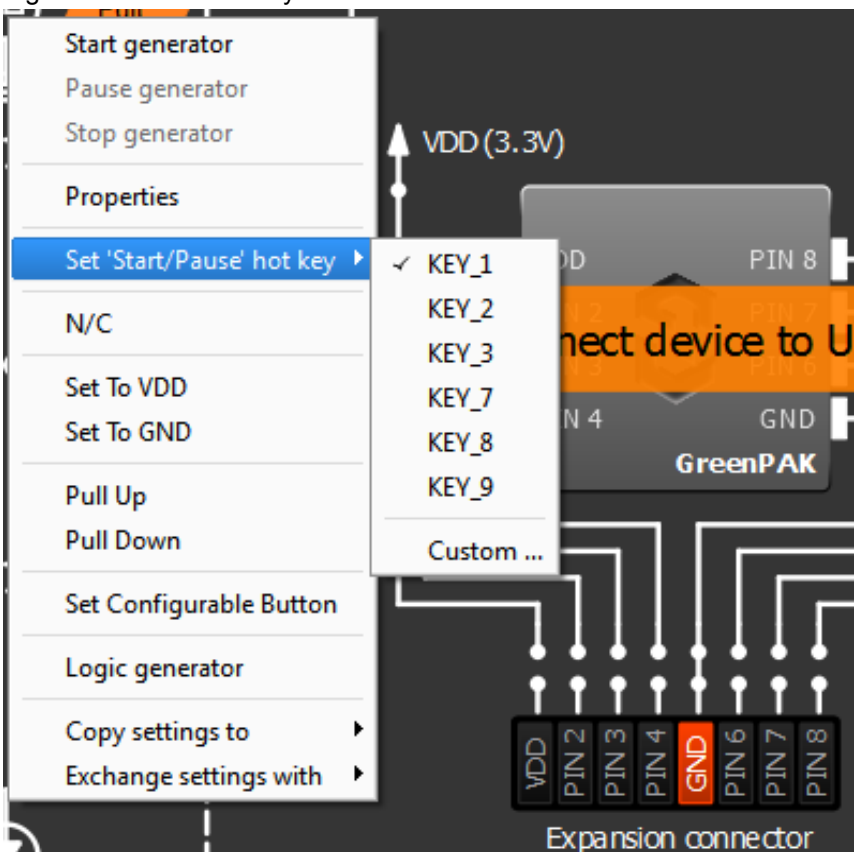


User can configure each connection. VDD/GND, High-Z or Pull Up/Down are available.

User can assign Hot Key for 'Push' action. The assigned key will simulate mouse click over the key.

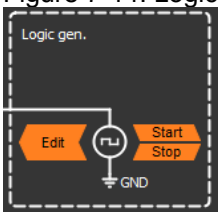
User can assign the same hot key to other Switches which will allow changing the key values of all the Switches with the same hot key at once (Figure 7-13).

Figure 7-13. Set Hot Keys



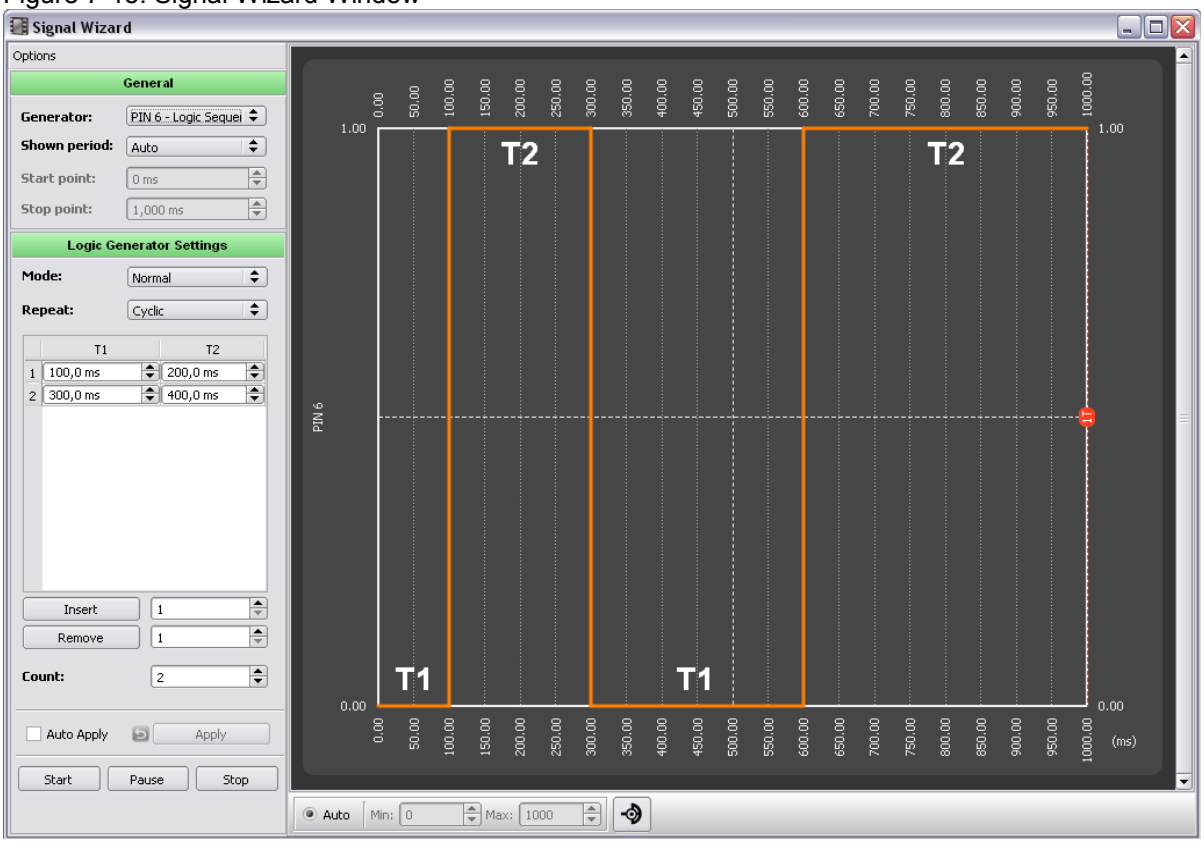
7.2. Generators
7.2.1. Logic Generator

Figure 7-14. Logic Generator



Logic generator is used for generating the logic pulses. 'Edit' button allows the user to configure the signal:

Figure 7-15. Signal Wizard Window

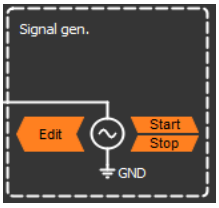


Configuration Options:

Mode:	Normal/Invert	- signal mode;
Repeat:	One shot/Cyclic	- repeat option;
T1/T2 Values Table:		- sets of pulses (T1 – low duration, T2 – high duration of one pulse)
Insert:		- insert pulse to the entered position;
Remove:		- remove pulse from the entered position;
Count:		- pulses count;

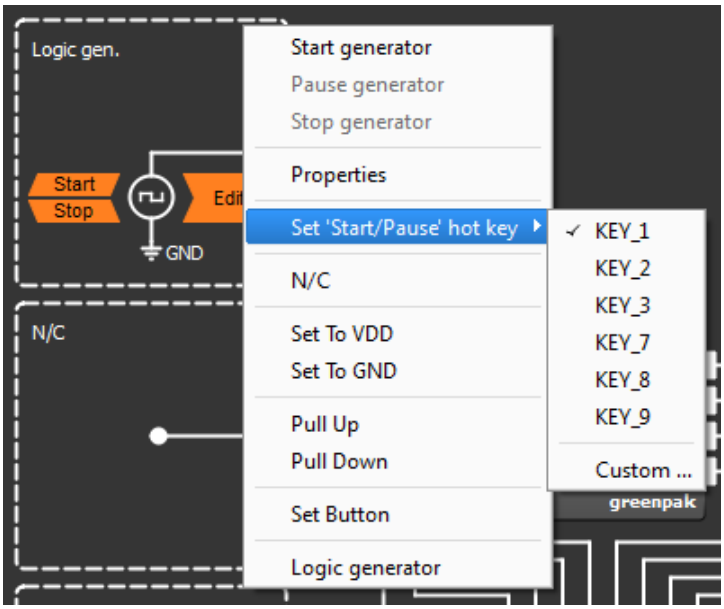
7.2.2. Signal (Analog) Generator

Figure 7-16. Signal Generator



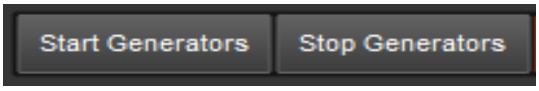
Signal generator is used to generate analog signals: Constant Voltage level, Saw, Triangle, Trapeze (Trapezoid), Sine, User defined.
Logic and signal generators can be started/paused/stopped using orange buttons or through the context menu. The user can also assign hot keys for start/pause.
Several generators can use the same hot key to start/pause at once. This is the right way to start more than one generator at the same time.

Figure 7-17. Start/Pause Hot Key



The ‘Start Generators’ and ‘Stop Generators’ buttons can also be used in this way:

Figure 7-18. ‘Start Generators’ and ‘Stop Generators’



Signal Generator settings:

Type: Const voltage level/Trapeze/Sine/User Defined - type of waveform;

Constant value:

U: - voltage level;

Figure 7-19. Generators Settings

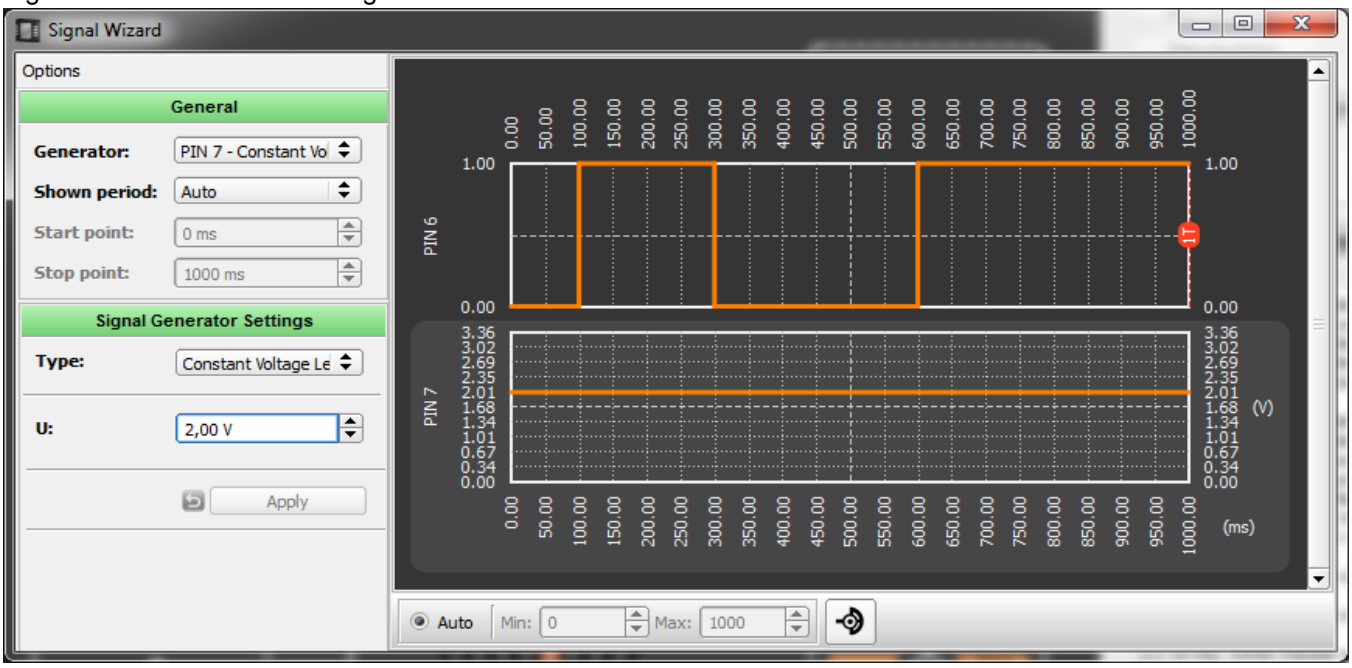
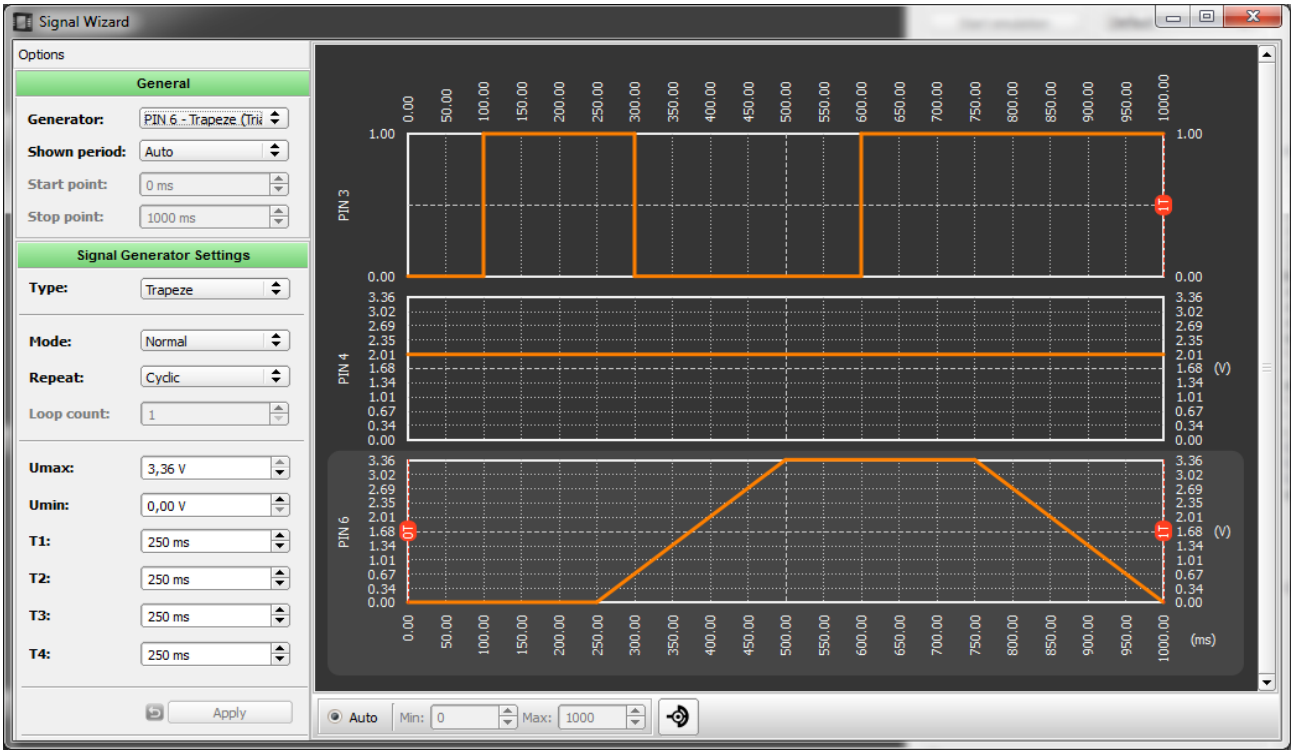


Figure. 7-20. Trapeze (Trapezoid)



Trapeze settings:

Mode:	Normal/Invert	- signal mode
Repeat:	One shot/Cyclic	- repeat option;
Umax/Umin		- max/min voltage level
T1, T2, T3, T4		- duration of trapeze

Figure 7-21. Duration of Trapeze (Trapezoid)

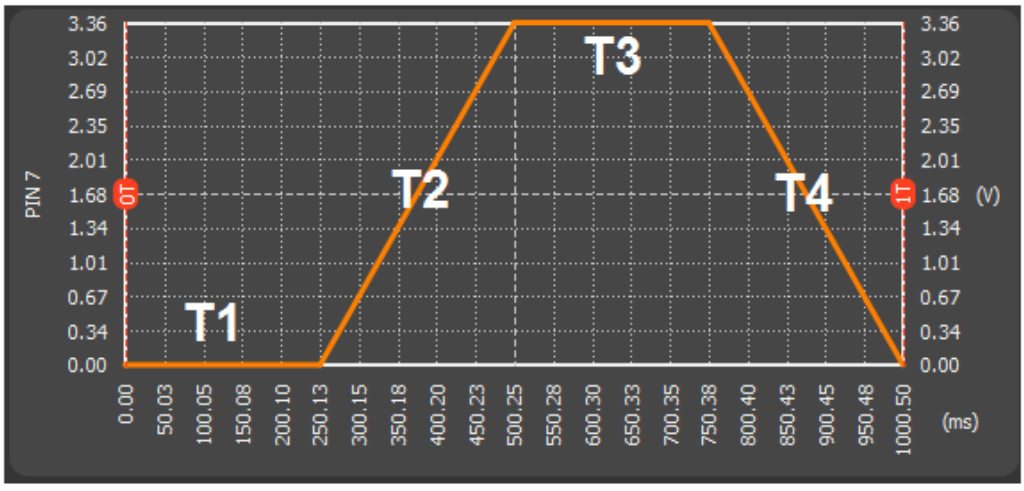


Figure 7-22. If T3 = 1: Signal is a Triangle

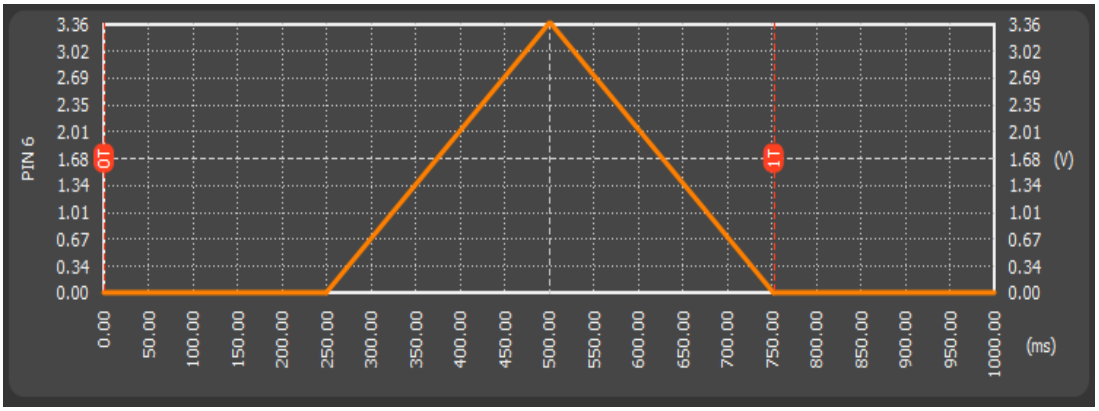


Figure 7-23. If T3 = 1 and (T2 = 2 or T4 = 2): Signal is a Sawtooth

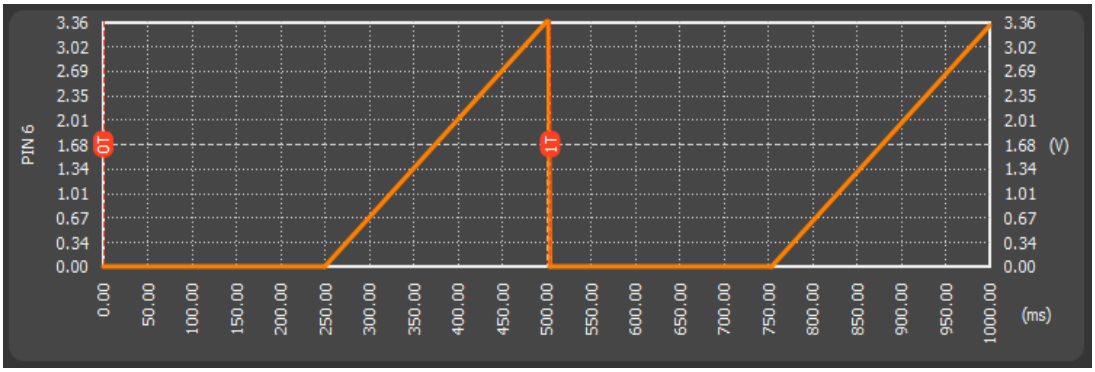
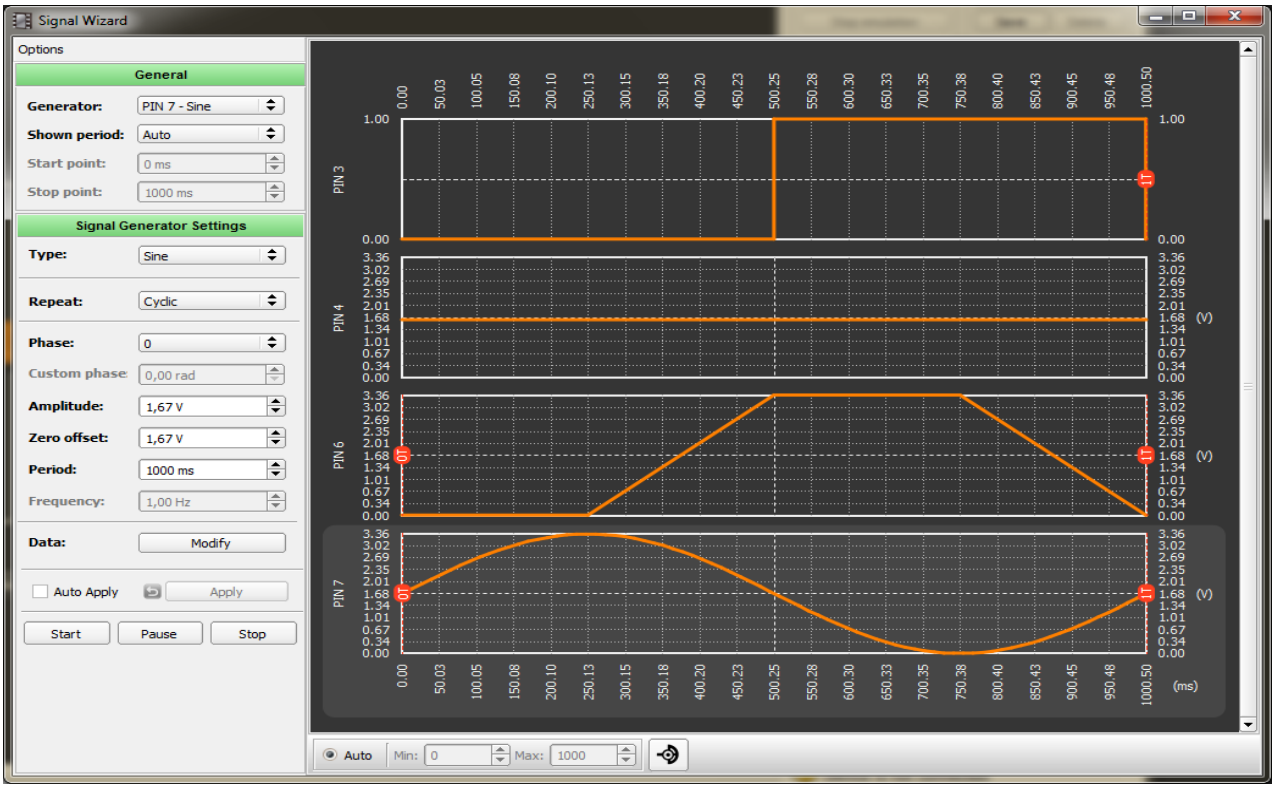


Figure 7-24. Sine

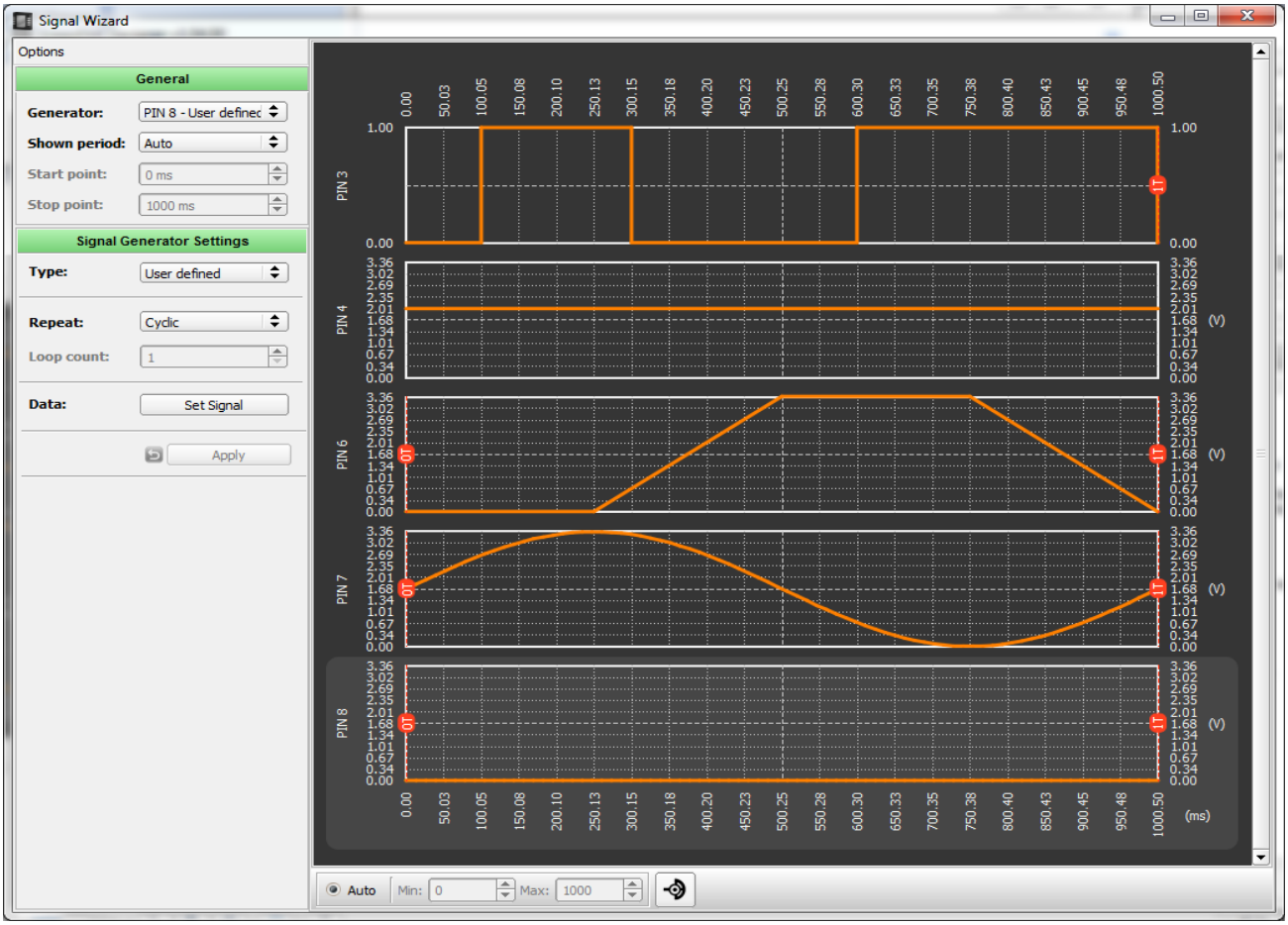


Sine settings:

Repeat:	One shot/Cyclic	- repeat option
Phase:	Custom/0/Pi:2/Pi/3Pi:2	- φ0
Amplitude:		- amplitude
Zero offset:		- zero offset
Period:		- period
Data:		- change signal using Custom Signal Wizard
Custom phase:		- show phase in radian
Frequency:		- show frequency

7.2.3. User-Defined Generator

Figure 7-25. User-Defined Waveform

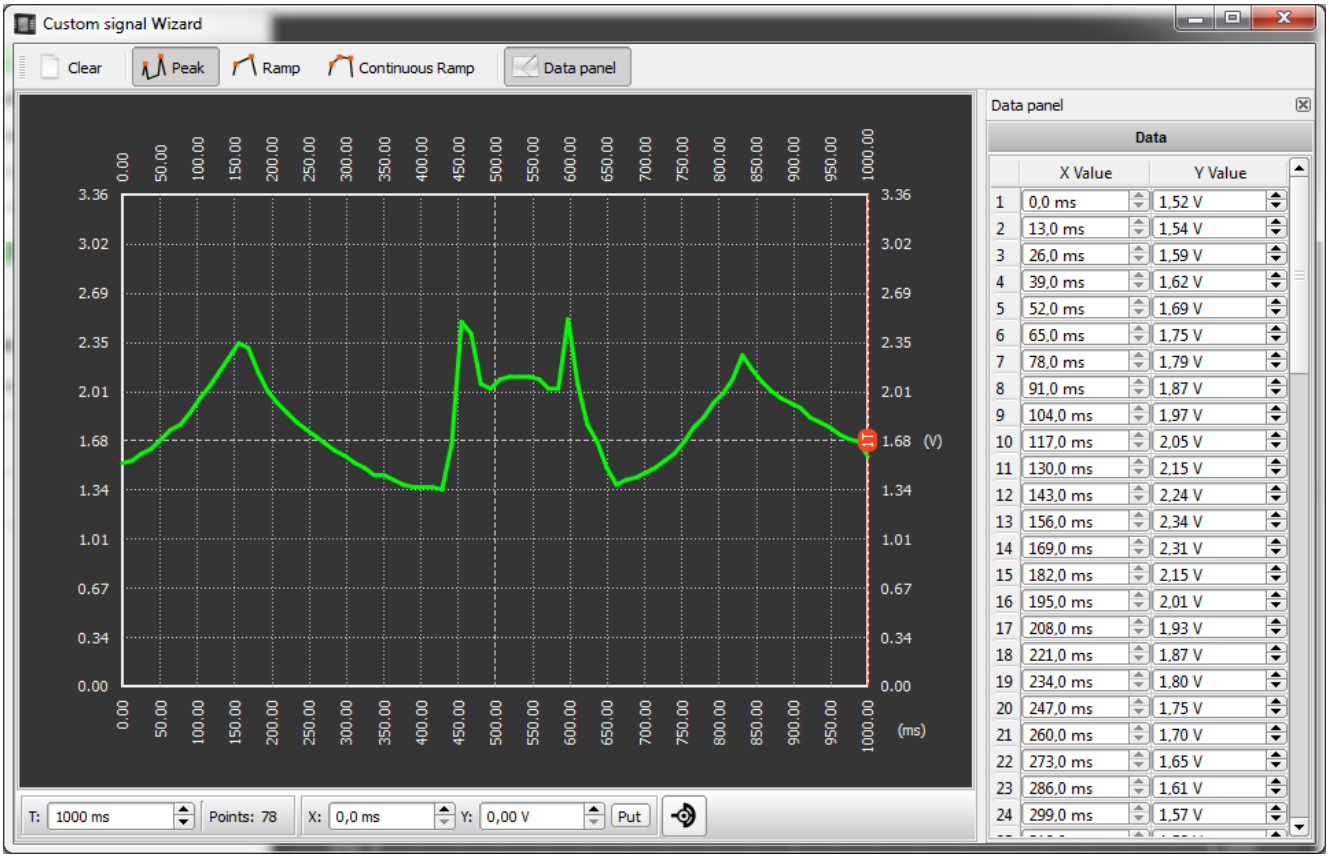


User-Defined Waveform Settings:

Repeat: One shot/Cyclic - repeat option;

Data: - change signal using Custom Signal Wizard

Figure 7-26. Custom Signal Wizard (Arbitrary waveform)



Toolbar:

Clear	- clear data
Peak/Ramp/Continuous Ramp	- draw modes
Data panel	- turn on/off the data table

Figure 7-27. Peak

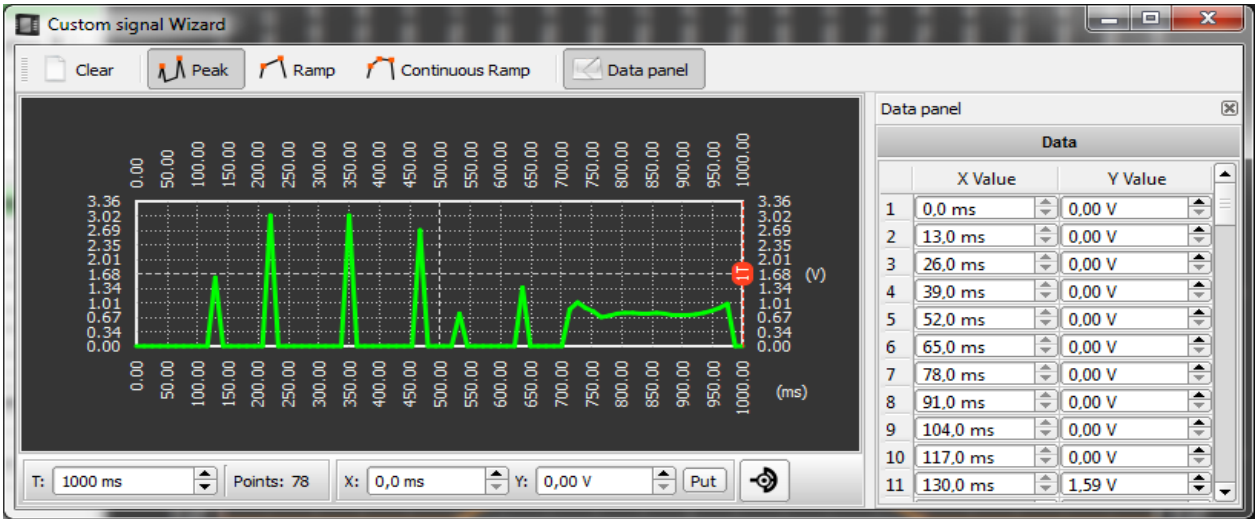


Figure 7-28. Ramp

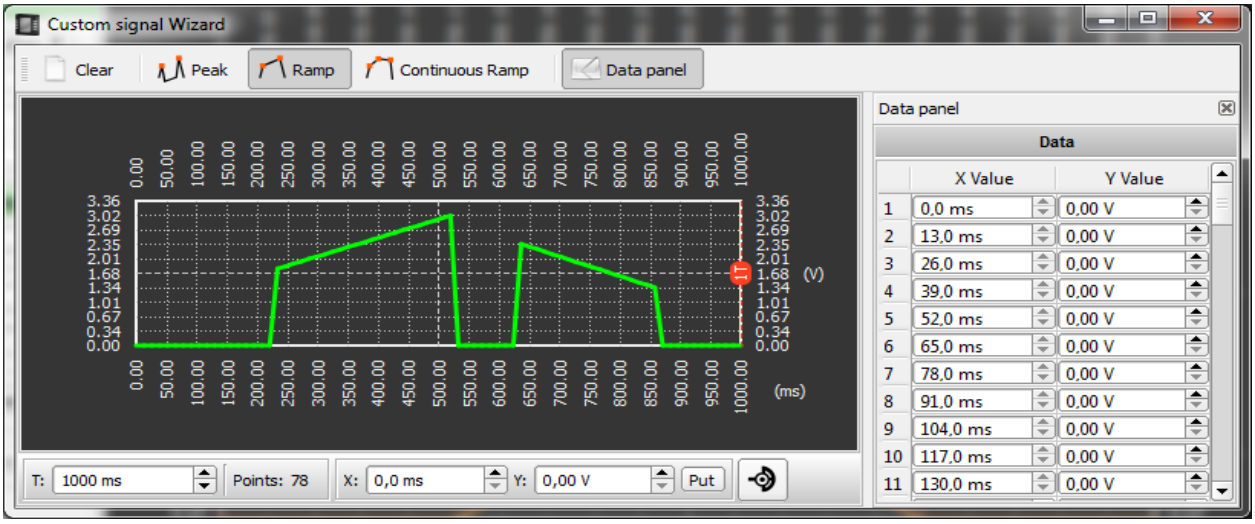


Figure 7-29. Continuous Ramp

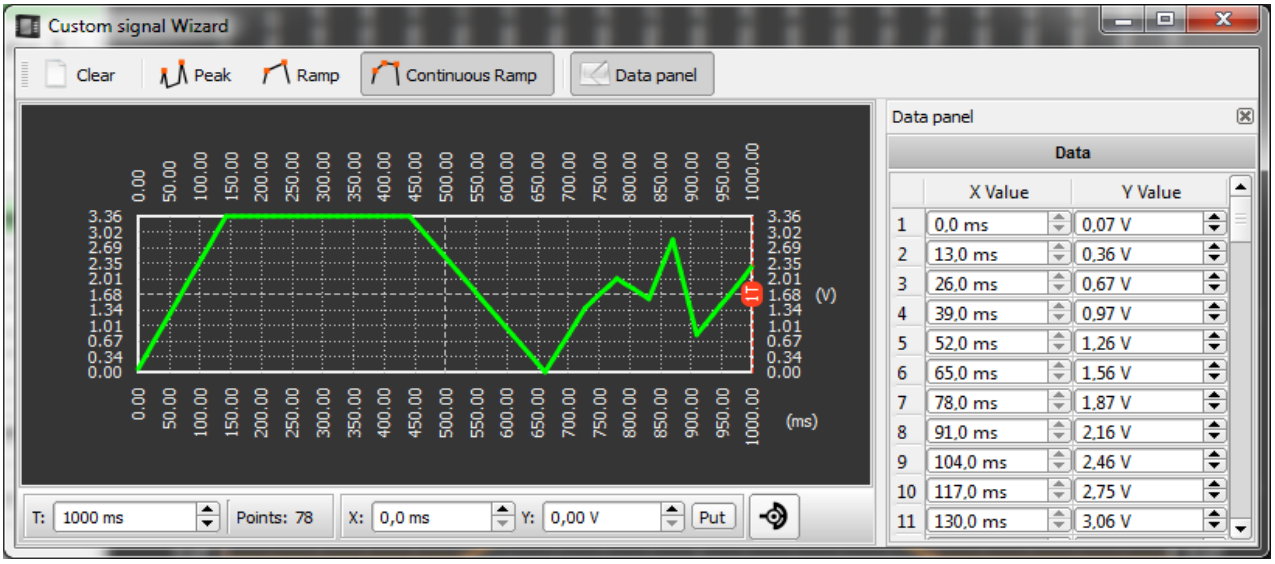


Figure 7-30. Data Panel

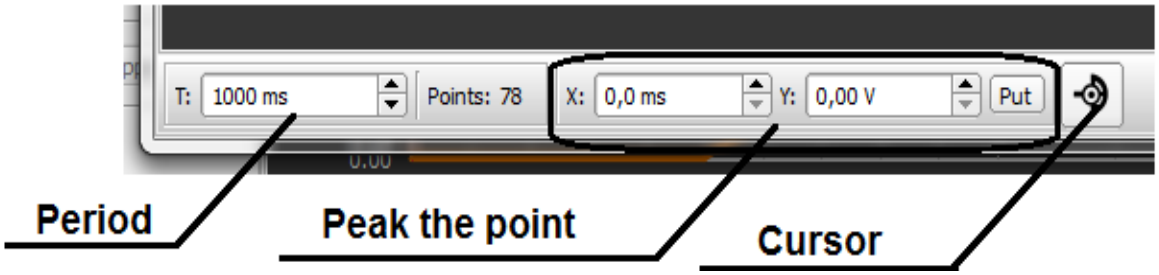
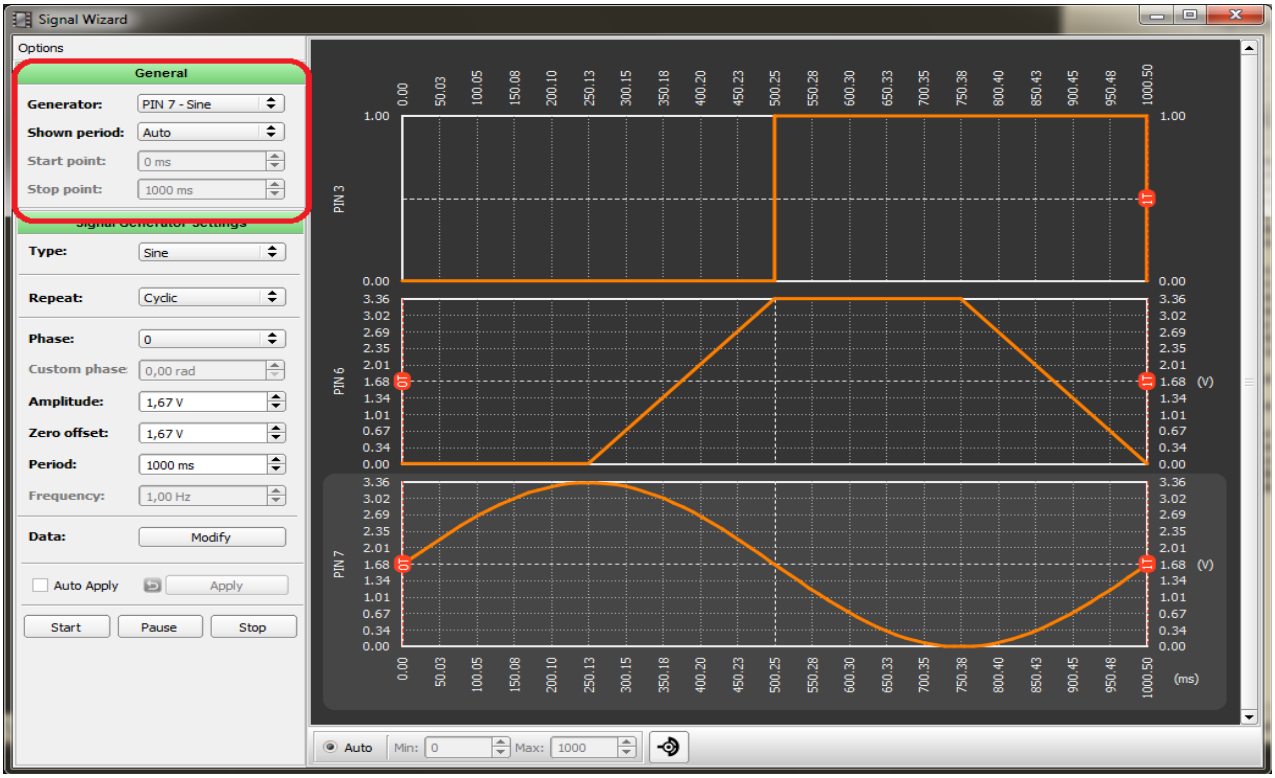


Figure 7-31. Cursor

7.3. General Options in a Signal Wizard Mode

Figure 7-32.General Options



General Settings:

Generator: - generator selector

Shown period: Auto/Custom/1T/2T/3T/4T - set the period of a current generator to be displayed

Start point: - start point generating signal

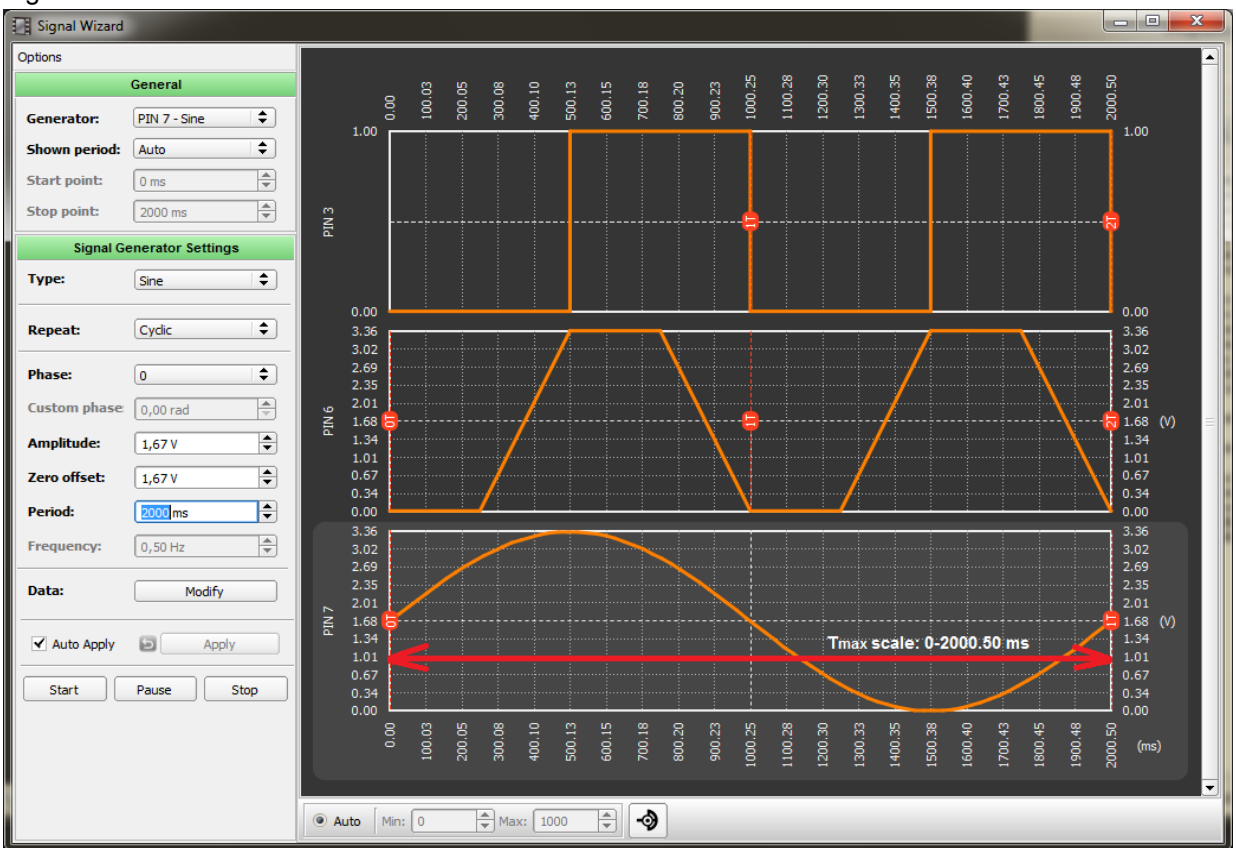
Stop point: -stop point generating signal

7.4. Period Modes

AUTO Mode

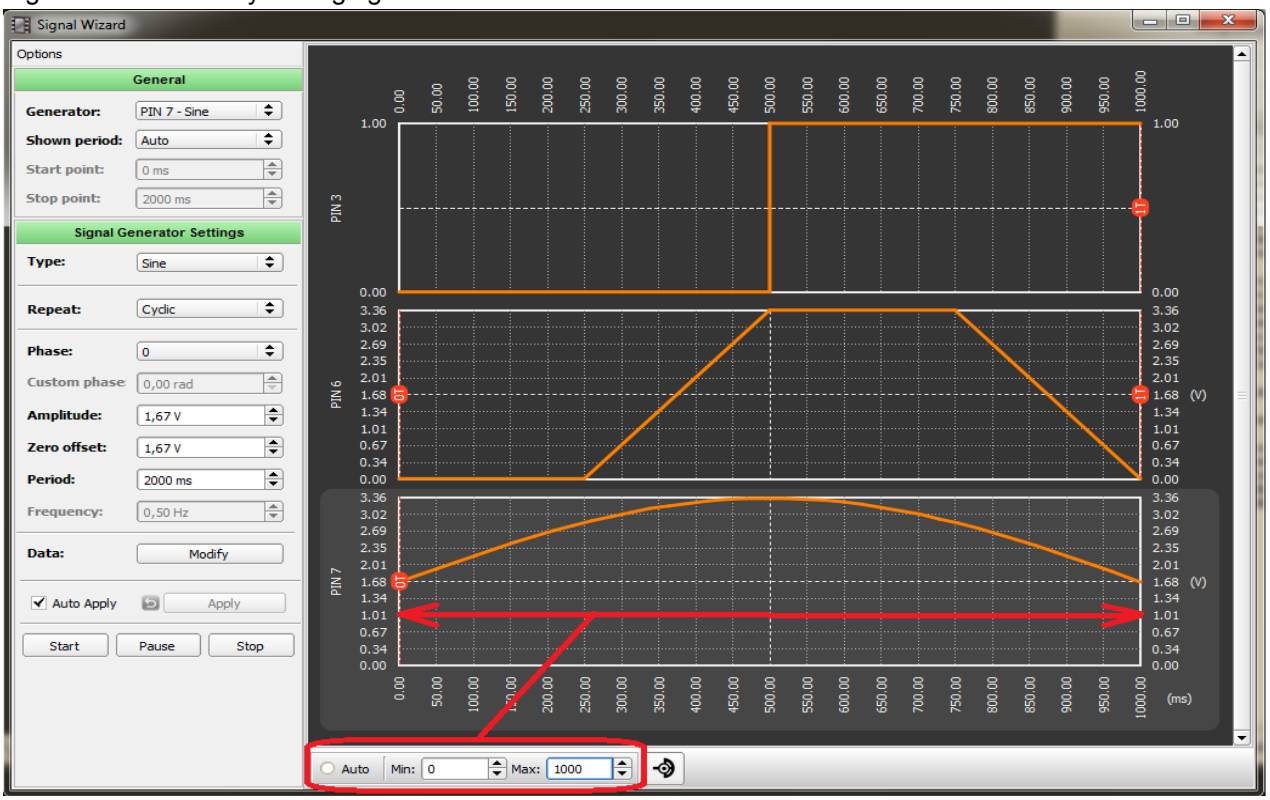
All generators with 'AUTO' option have one scale; this scale = MAX period of all generators with 'AUTO' option.

Figure 7-33. Auto Mode



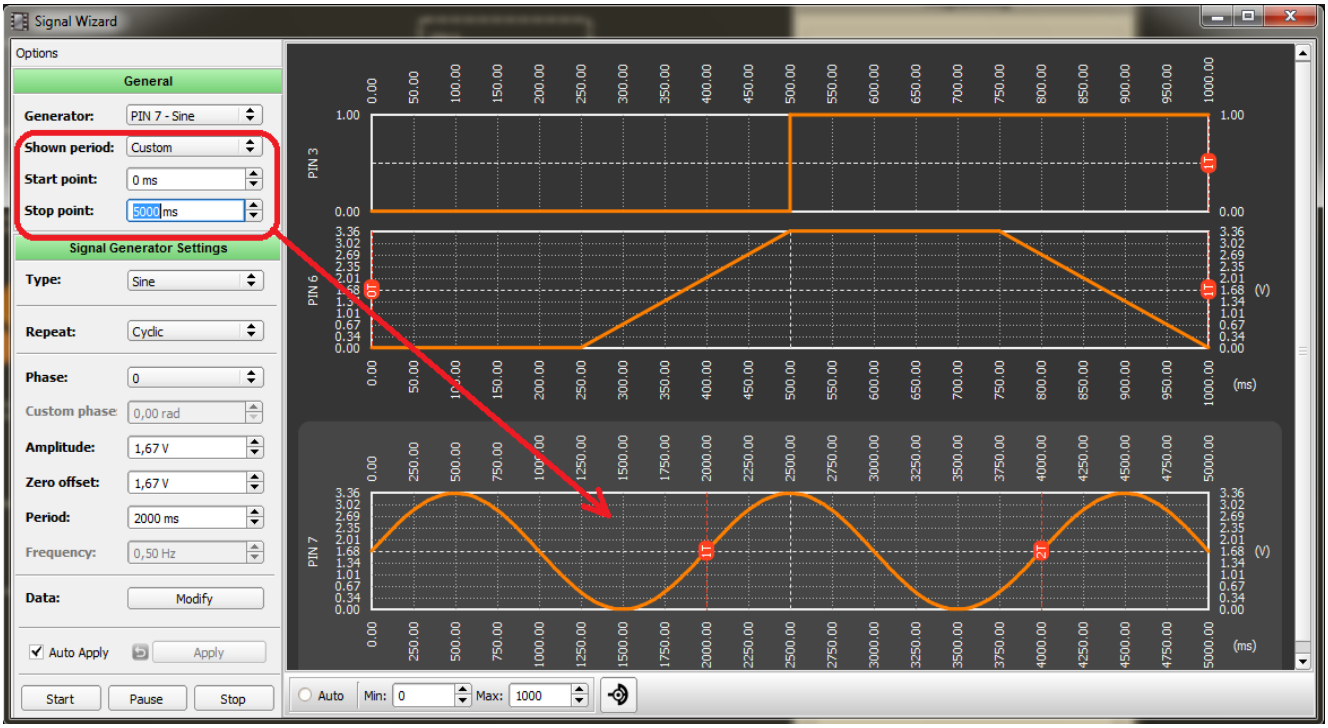
The user can manually change the scale.

Figure 7-34. Manually Changing Scale



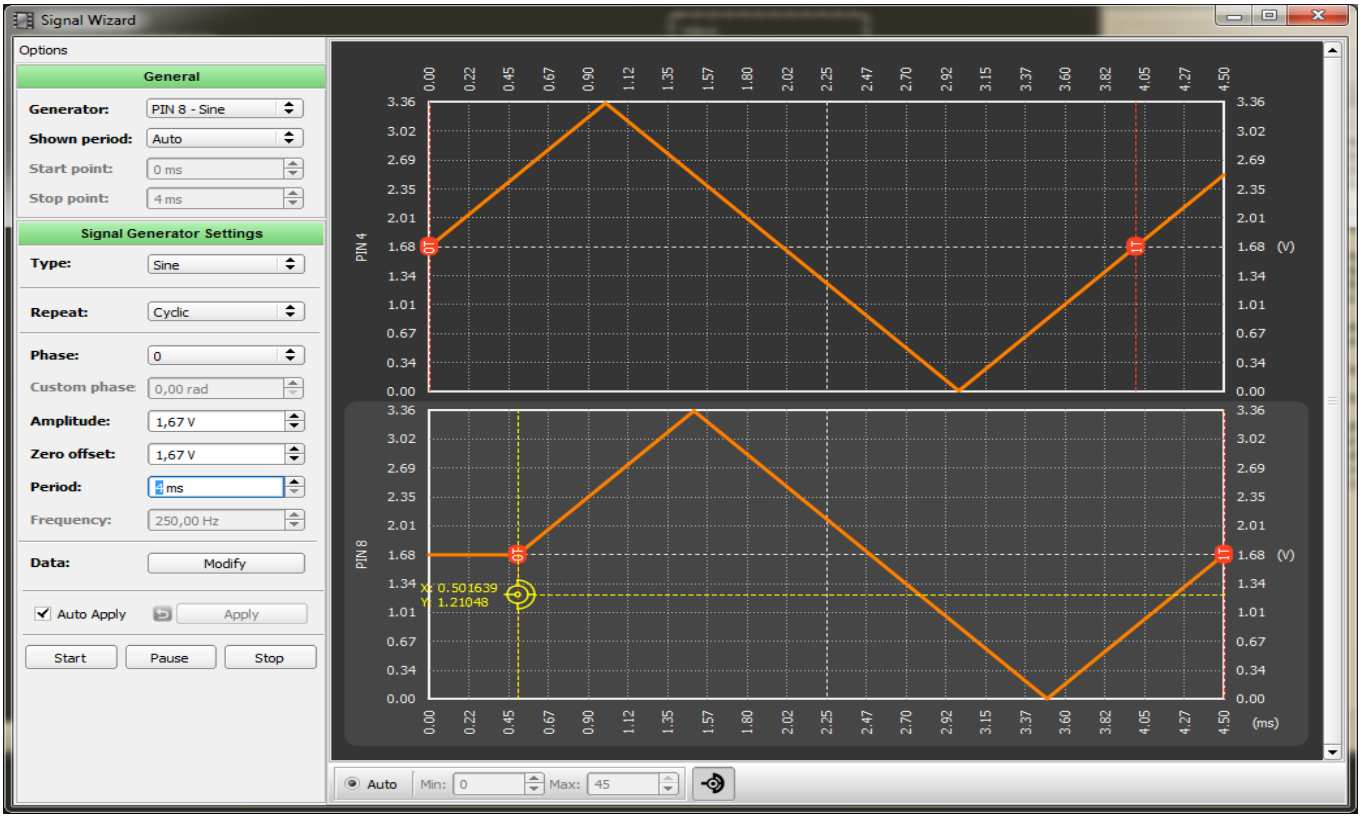
CUSTOM Mode.

Figure 7-35. Set Custom Period



The user can set a custom period to be displayed for any generator.
Note: Analog generators connected to PIN7 and PIN8 start generation 0.5ms later than those connected to PIN4 and PIN6. This delay is displayed on the graphs in a Signal Wizard when the AUTO mode is ON.

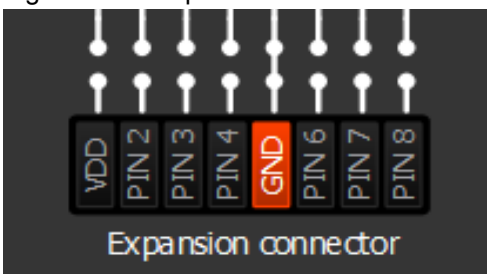
Figure 7-36. The Delay of Analog Generator



7.5. Expansion Connector

User can connect/disconnect I/O pads of GreenPAK with the expansion connector on the board.

Figure 7-37. Expansion Connector



7.6. Control Panel

Emulation:

Start emulation – load project to the chip and start the emulation;
Stop emulation – stop the emulation;

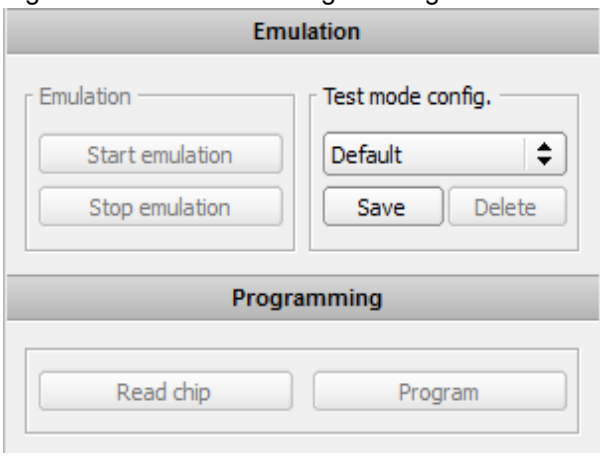
Test Mode Configuration:

The user can save current configuration of a test mode to the project file;

Programming:

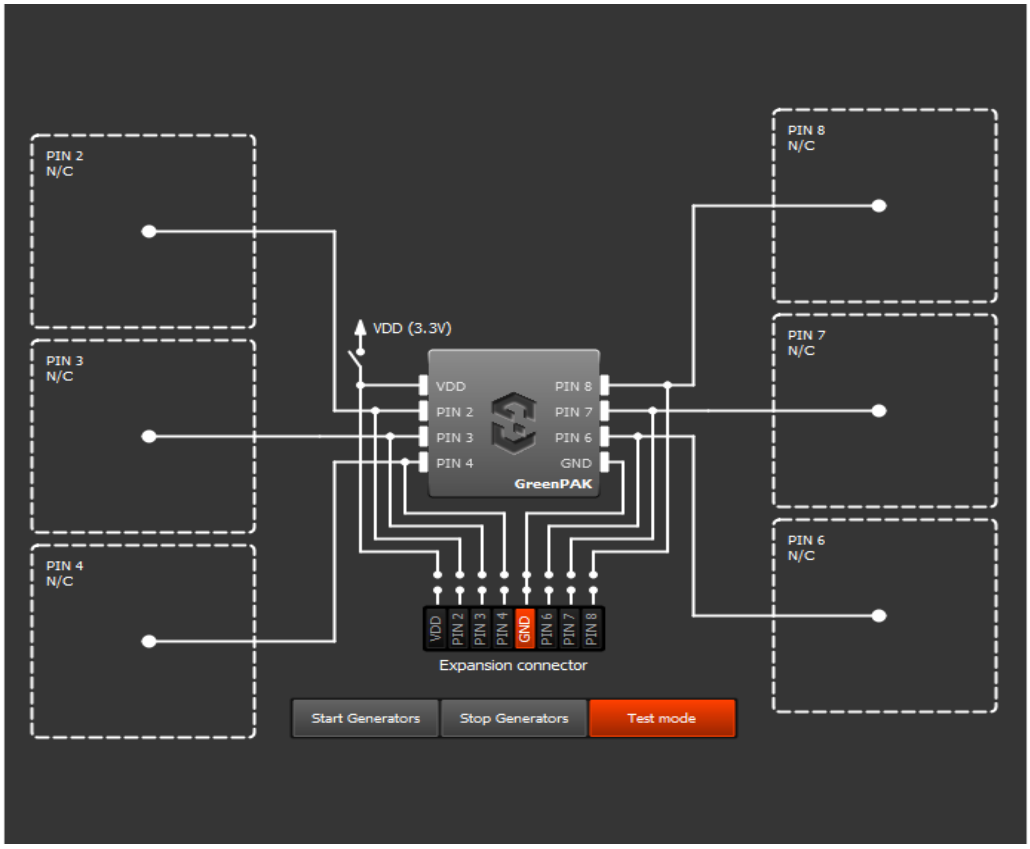
Read/Program chip with the current project using the emulation board;

Figure 7-38. Emulation/Programming



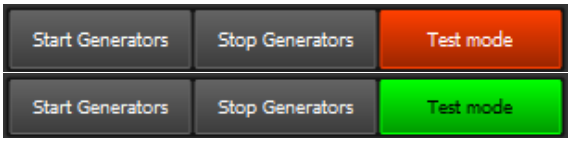
7.7. Test Mode and Emulation Process

Figure 7-39. Test Mode



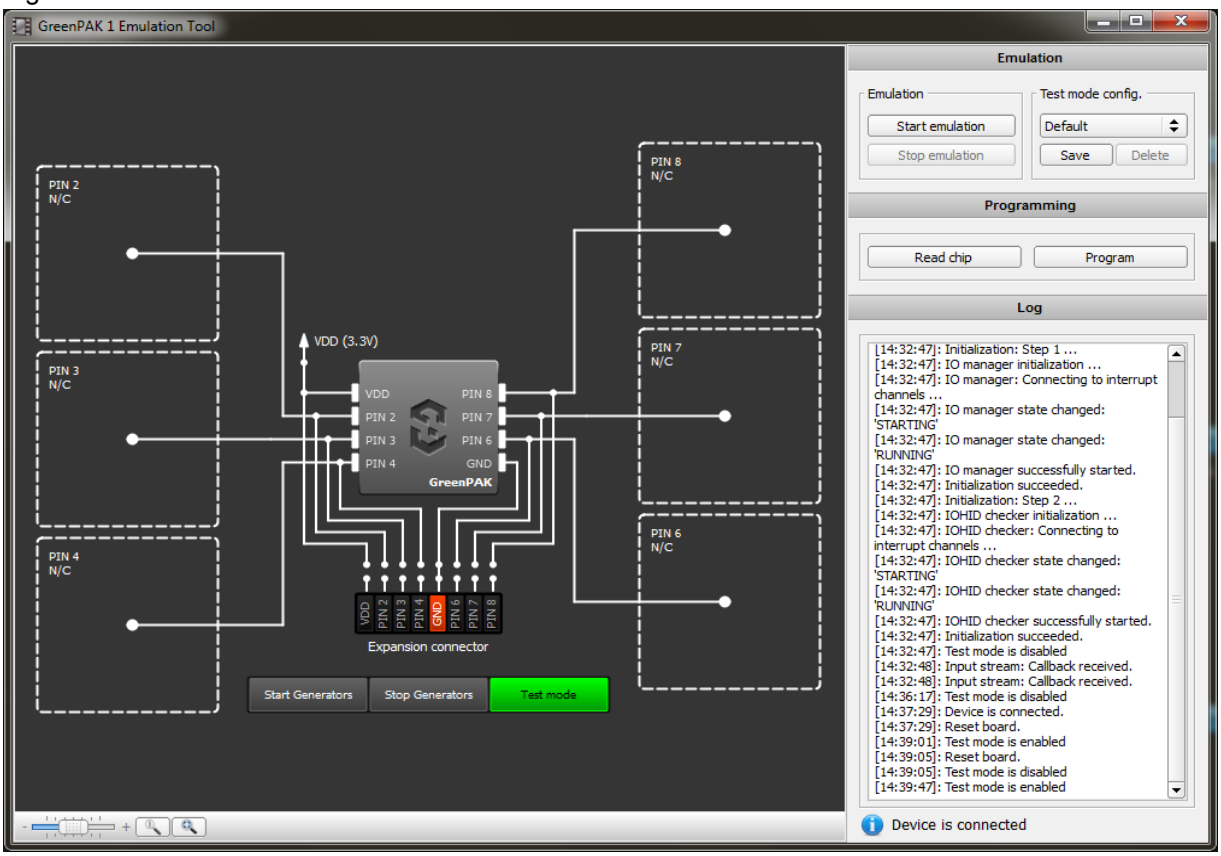
'Test mode' button is used for turning on/off the test mode.

Figure 7-40. 'Test mode' Button



Test mode can be used for connecting or disconnecting a chip's I/O pads to stimulus areas, configured by the user. The representation of test mode is illustrated below.
Emulation process can be started with the "Start emulation" button and will be indicated with the white logo in GreenPAK.

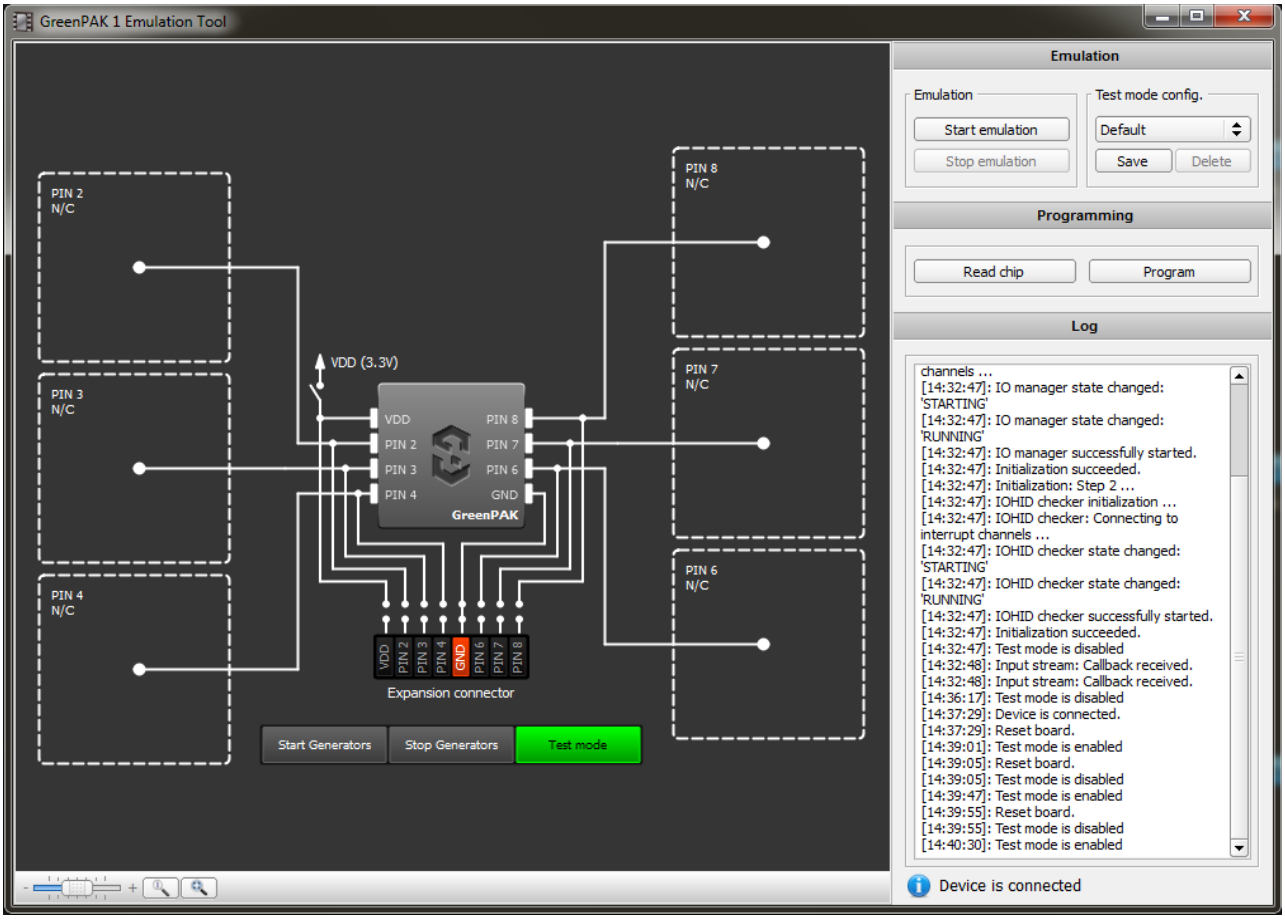
Figure 7-41. Start Emulation



In the emulation mode, the test mode will be automatically turned on. The current project will be loaded (but not programmed) to the chip, and will be ready for test on the emulation board. The user can change any configuration during the emulation process.
Note: Power turns on when Emulation goes on. The Power key must be turned on in emulation mode to send power to the chip, otherwise the emulation will not work. Power turns off when Emulation goes off.

The user can check the programmed chip using the test mode without emulation. In order to do this, turn on the test mode and the Power key. The test mode can work without power on the chip. The user will control the Power key manually.

Figure 7-42. Using Test Mode Without Emulation



8. GreenPAK 2 Emulation Board

Figure 8-1. The Main Screen

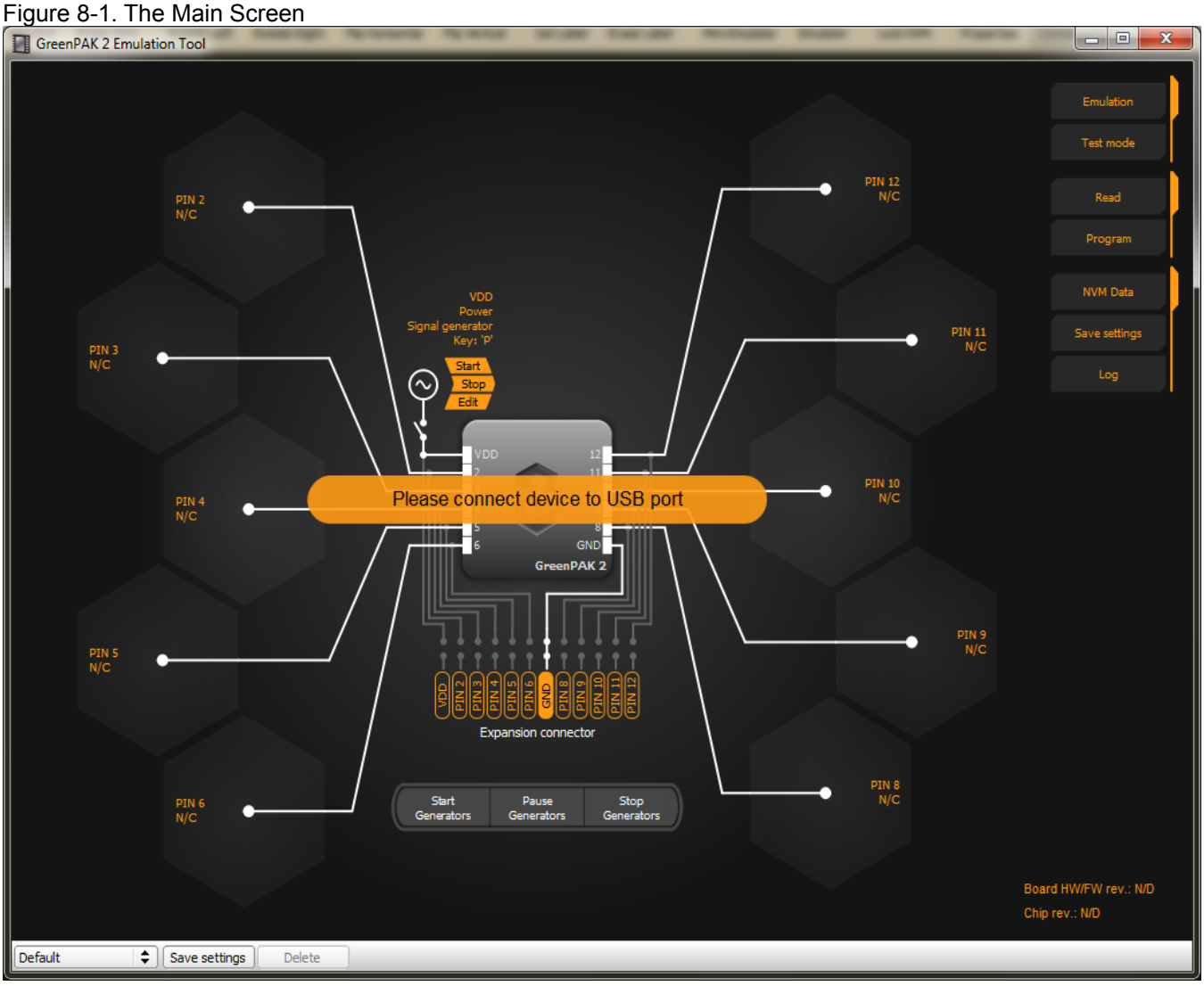
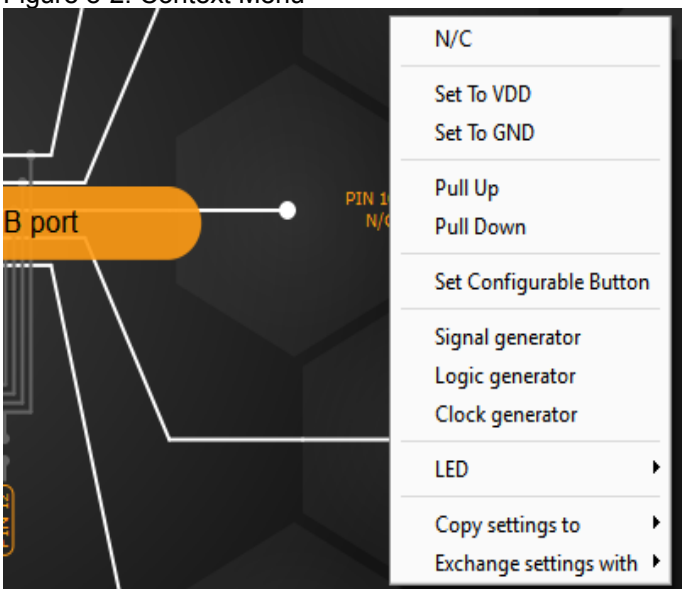


Figure 8-1 displays the GreenPAK IC with dotted areas, and expansion connectors which are connected to pins. The right bottom corner displays revision information.

Dotted areas are used to configure input connections. Use the context menu to manage them.

Figure 8-2. Context Menu



Copy settings to... – allows the copy settings from the current area to another connection.
Exchange settings with... – exchange settings of the current area with another connection.

8.1. Types of Areas

Fixed Inputs(figure 8-3 – 8-7)

Figure 8-3. N/C (not connected)

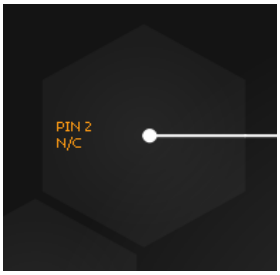


Figure 8-4. Set to VDD

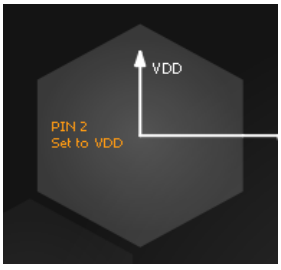


Figure 8-5. Set to GND

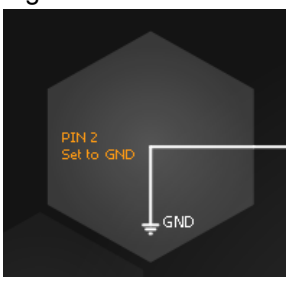


Figure 8-6. Pull Up

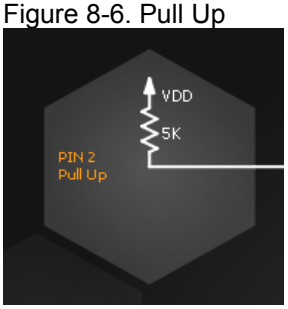
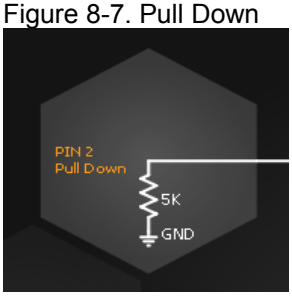


Figure 8-7. Pull Down



LED's(Figure 8-8, 8-9)

Figure 8-8. Inverted Buffered LED, Inverted Buffered LED+Pull Up, Inverted Buffered LED+Pull Down

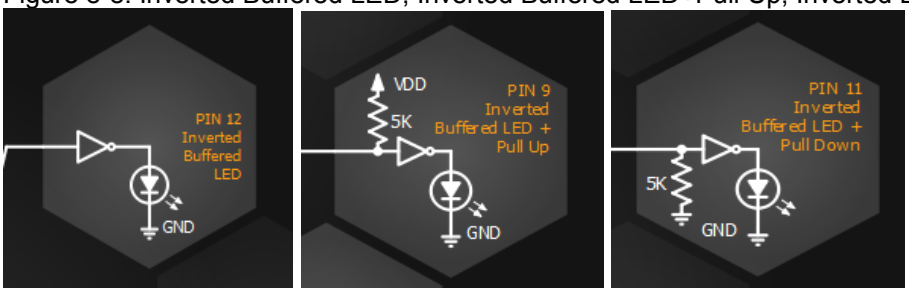
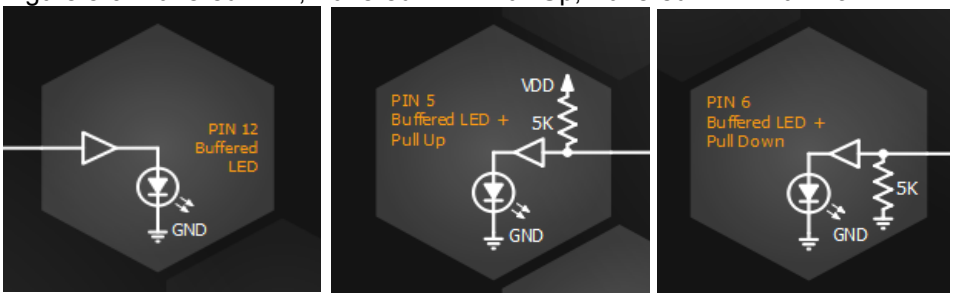
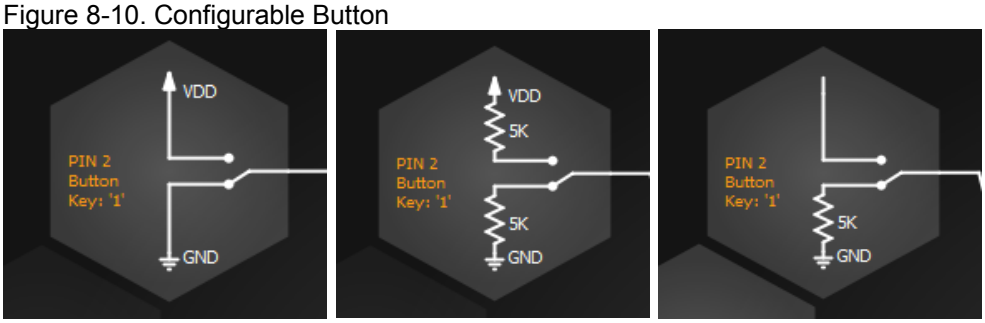


Figure 8-9. Buffered LED, Buffered LED+Pull Up, Buffered LED+Pull Down



Configurable Input (Figure 8-10)

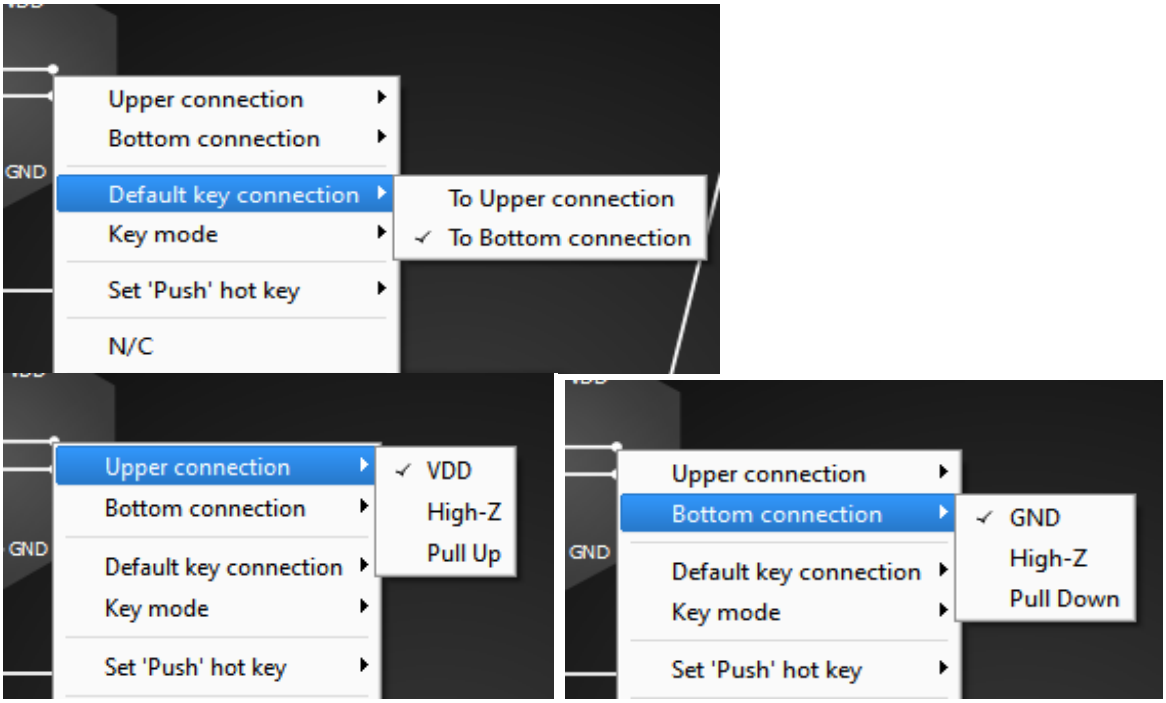
Figure 8-10. Configurable Button



The default connection can be set to either Upper connection or Bottom connection. Click your mouse over the key to change the value.

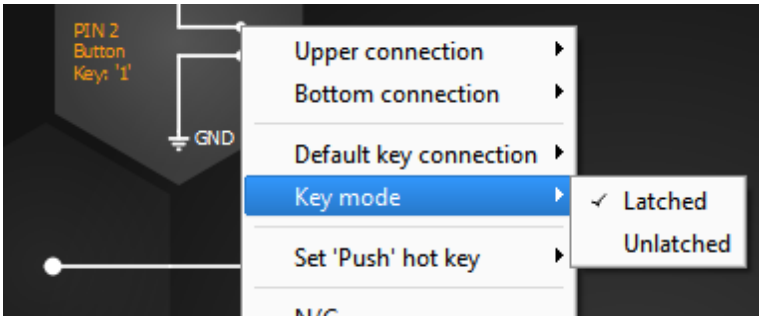
User can configure each connection to VDD/GND, High-Z or Pull Up/Down.

Figure 8-11. Default Key Connection.



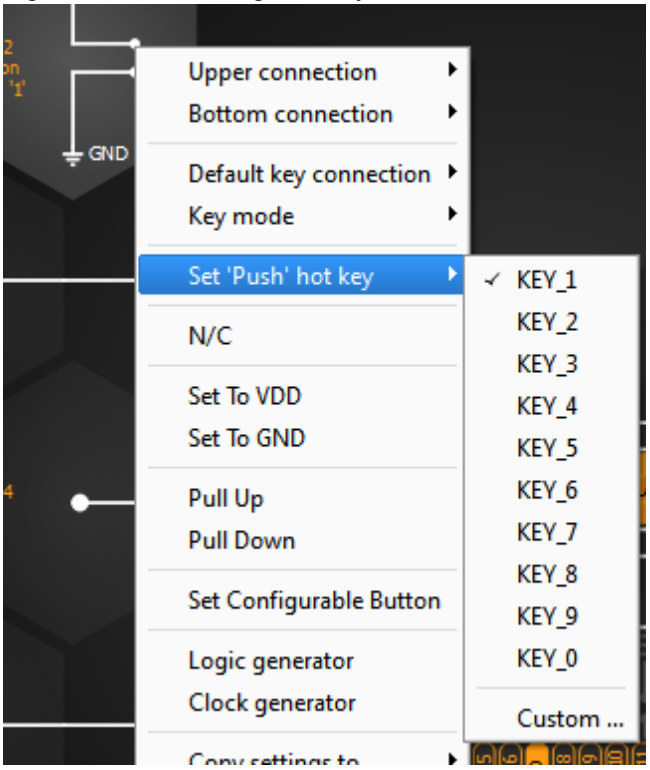
The switch has 2 modes: Latched or Unlatched, which can be configured from the context menu:

Figure 8-12. Key Mode



User can assign Hot Key for 'Push' action. The assigned key will simulate mouse click over the key:

Figure 8-13. Choosing Hot Key

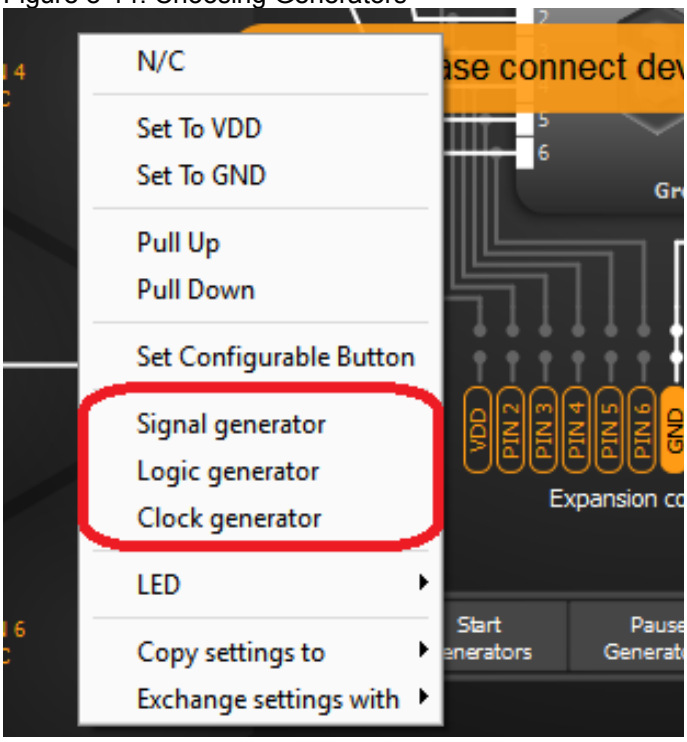


The user can assign the same hot key to multiple Switches, allowing a single hot key the ability to change the key values of all the Switches at once.

8.2. Generators

To each chip there can be connected 3 types of generators: Signal generator, Logic generator, and Clock generator.

Figure 8-14. Choosing Generators



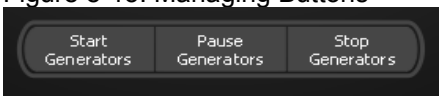
Each generator has its own settings. For the settings window to appear press the Edit button.

On the left, the options table is divided into 2 groups:

1. General – applied to all types of generators, and
2. Special for each generator.

To start the generators, use the buttons below the Emulator.

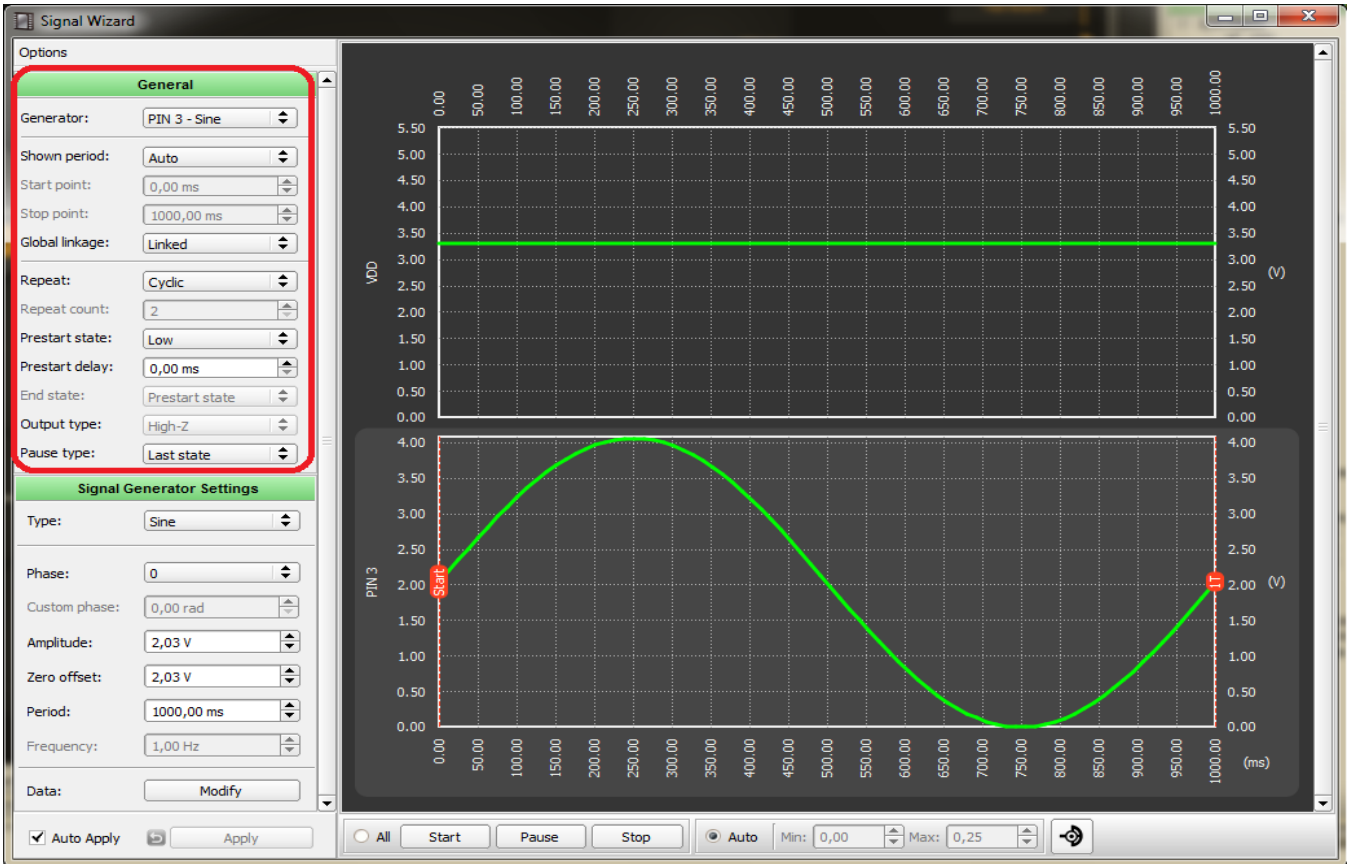
Figure 8-15. Managing Buttons



Note: These buttons can only be controlled by generators with an installed Global Linkage flag.

8.2.1. General Options in a Signal Wizard Mode

Figure 8-16. General Option



Generator:		- generator selector
Shown period:	Auto/Custom/1T/2T/3T/4T	- set the period of a current generator to be displayed
Global linkage	Linked/Unlinked	-if generator is linked, it will be controlled by buttons “Start”, “Stop” and “Pause” on the Emulator
Repeat	One shot/Cyclic/Custom	- repeat option
Prestart state	Low/Start point(V0)/High-Z	-state before start
Prestart delay		-delay before start
End state	Keep last state/Prestart state	-pin state after generation
Output type	High-Z/Strong Drive/Open Drain, Drives High/ Open Drain, Drives Low/Resistive Pull Up/ Resistive Pull Down/ Resistive Pull Up/Down	- type of output
Pause type	Last state/Low/High/High-Z	-hold state when it is paused

8.2.2. Period Modes

AUTO Mode

All generators with 'AUTO' option have one scale; this scale = MAX period of all generators with 'AUTO' option.

Figure 8-17. One Scale for All Generators

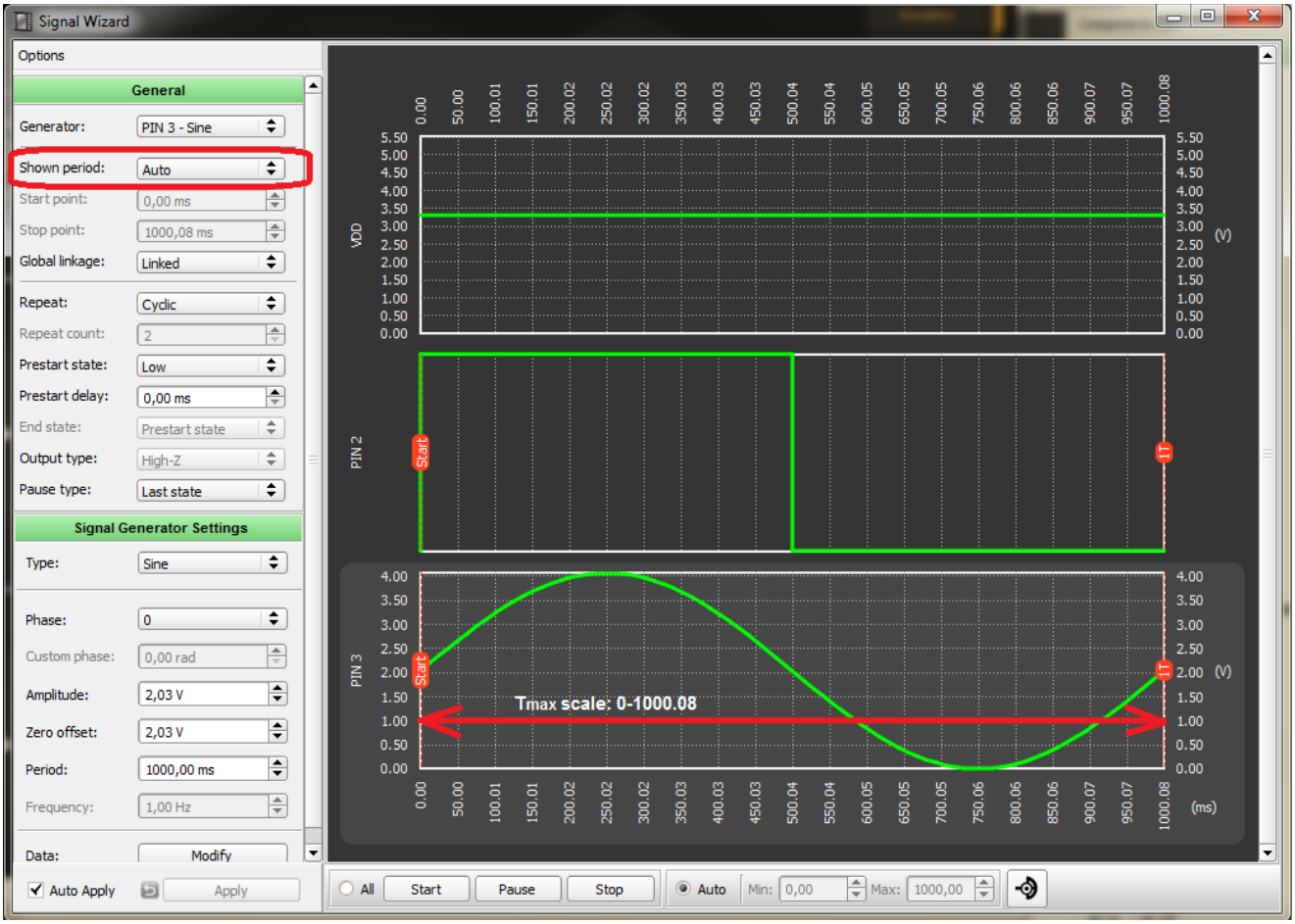
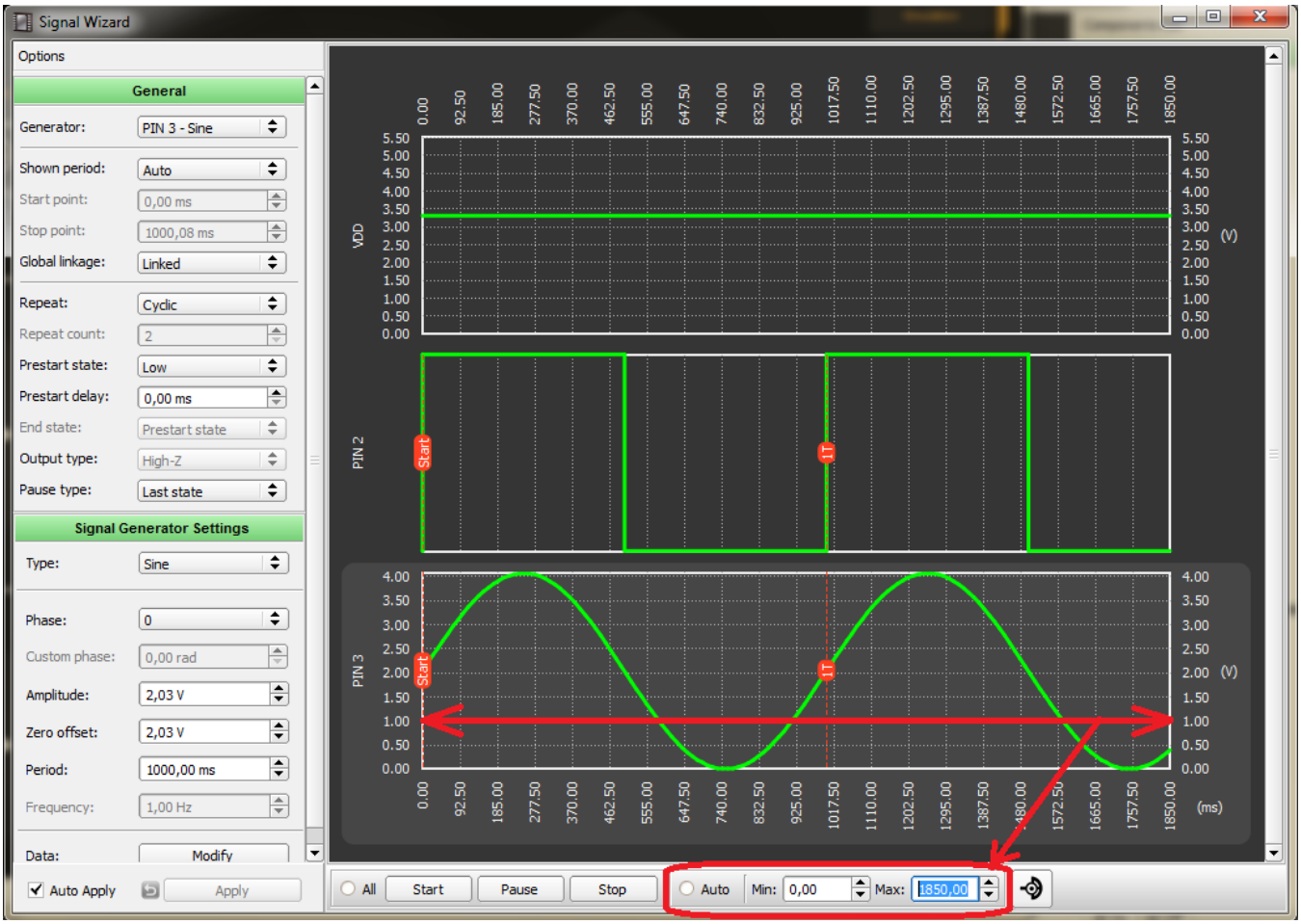


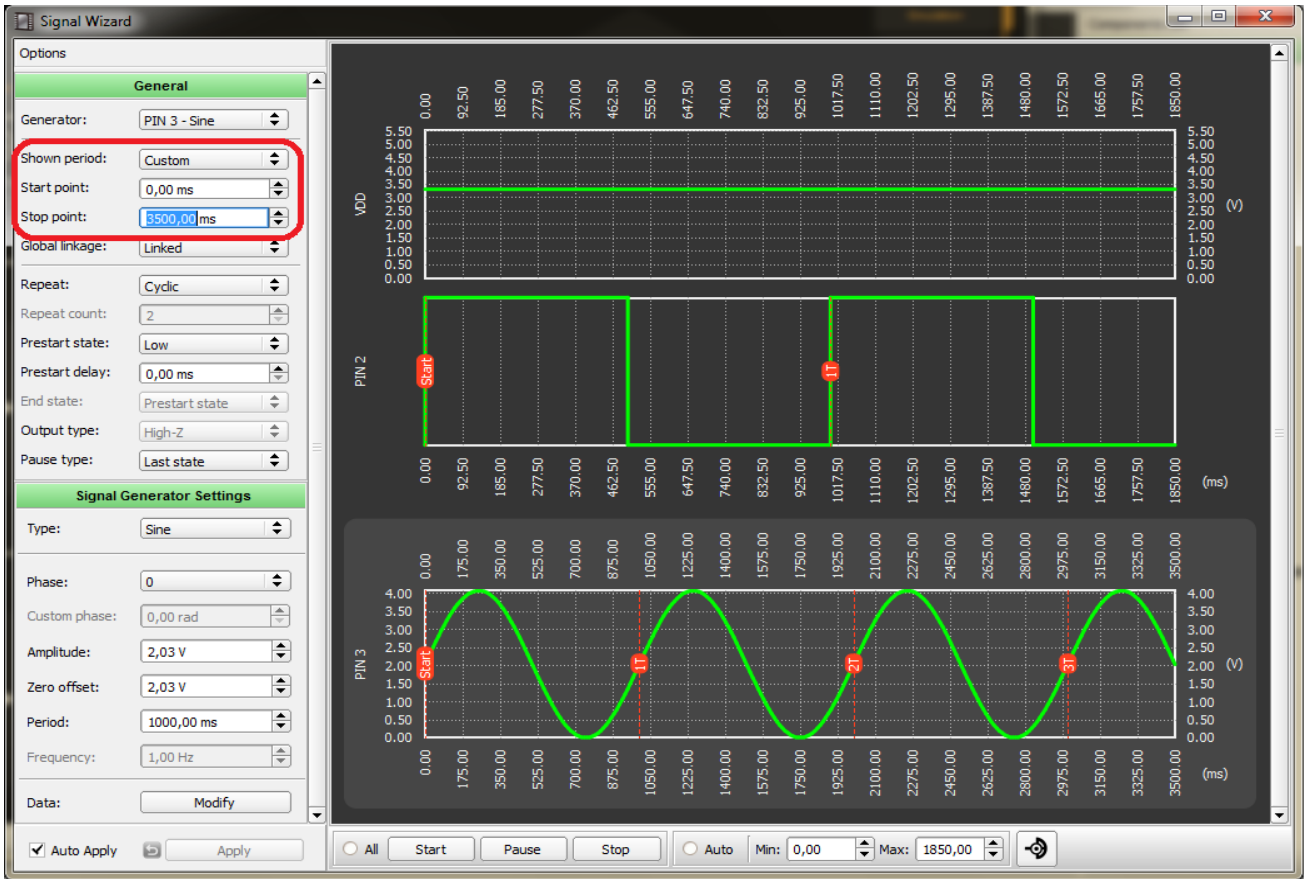
Figure 8-18. User Can Change the Scale Manually



button turns on/off the mouse coordinates on the timing diagrams.

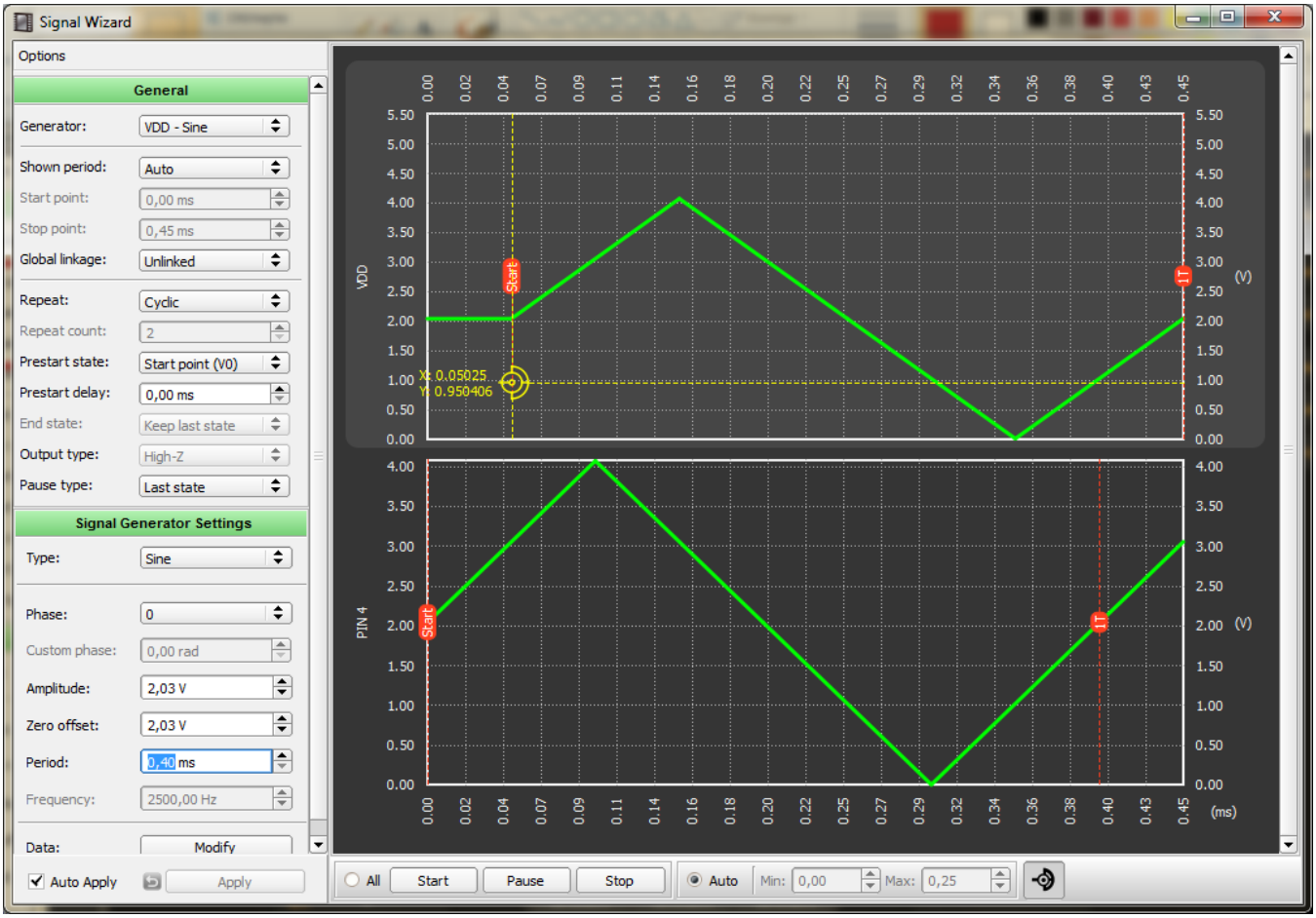
CUSTOM Mode

Figure 8-19. Choosing Period Options



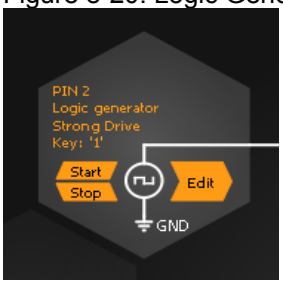
User can set a custom period to be displayed for any generator.
Note: Logic and clock generators have a 75 mks delay before start. The signal generator connected to PIN 8 or 9 has delay 25 mks before start. In case it is connected to PIN 1(VDD) or 11 the delay is 50 mks before start. This delay is displayed on the graphs in Signal Wizard when the AUTO mode is ON.

Figure 8-20. Start Delay



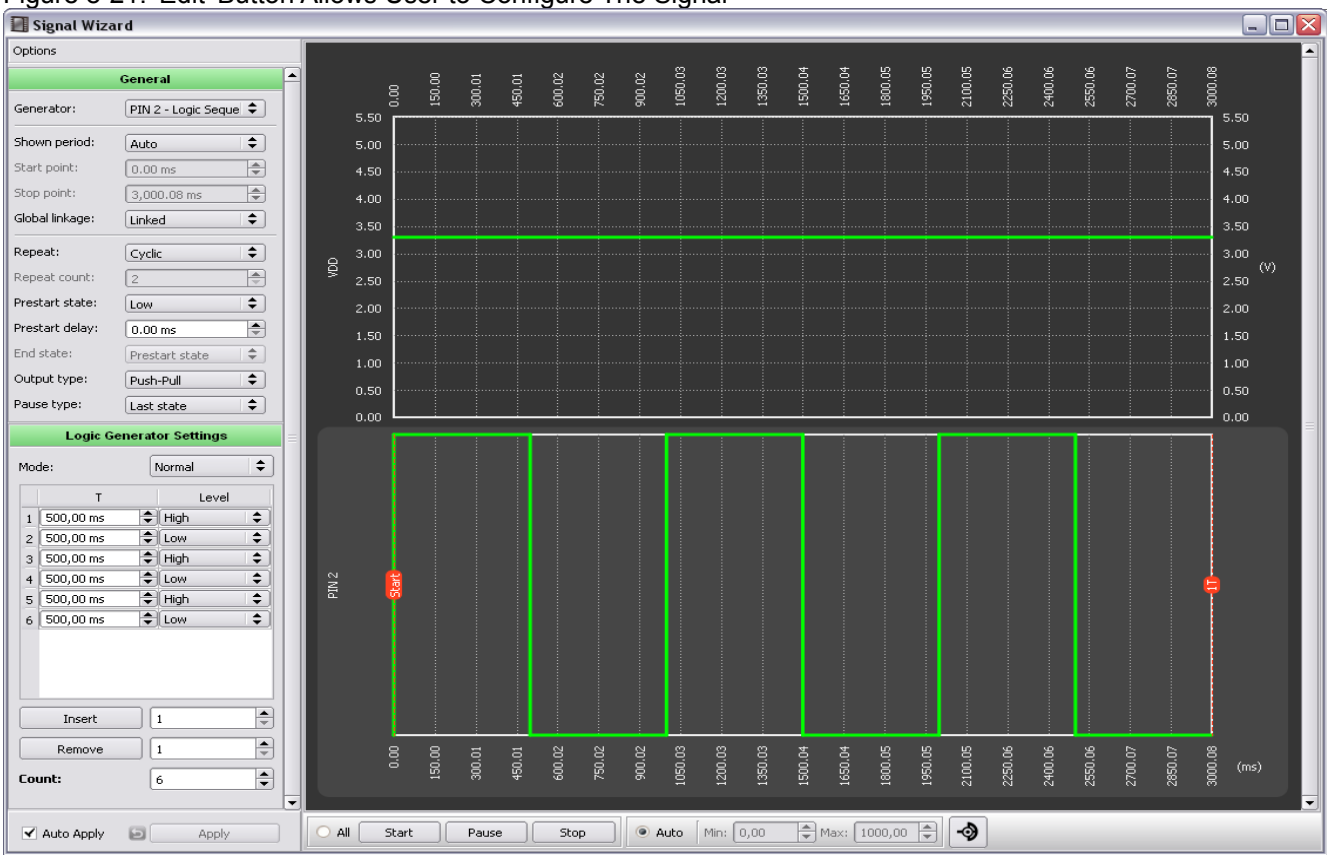
8.2.3. Logic Generator

Figure 8-20. Logic Generator



Logic generator is used for generating the logic pulses.

Figure 8-21. 'Edit' Button Allows User to Configure The Signal

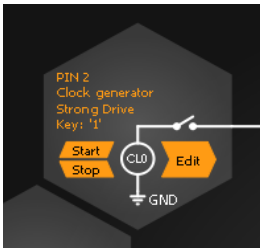


Configuration options:

Mode:	Normal/Invert	- signal mode
Repeat:	One shot/Cyclic/Custom	- repeat option
T/Level:		- sets duration of level
Insert:		- insert pulse to the entered position;
Remove:		- remove pulse from the entered position;
Count:		- pulses count

8.2.4. Clock Generator

Figure 8-22. Clock Generator

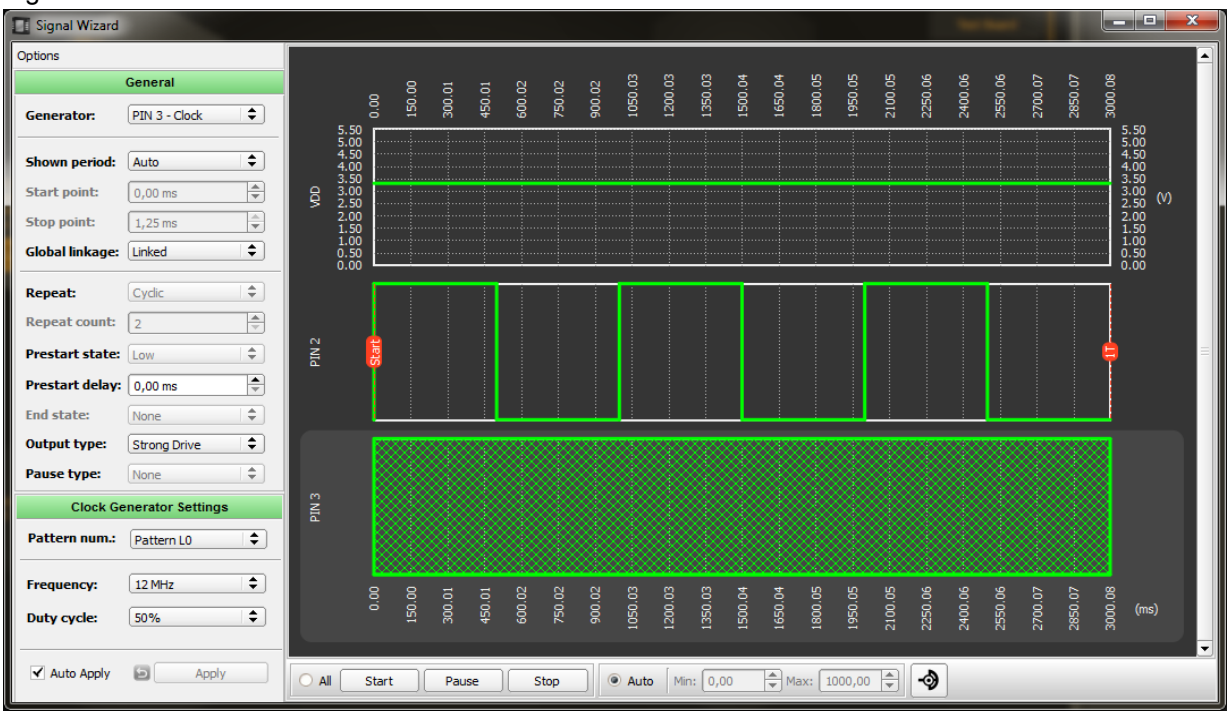


A high-frequency logic generator, which generates a 12 MHz frequency signal can be connected to any pin. Each Clock generator should be connected to its pattern (collection of generators' settings). There are 6 total patterns: L0/L1/L2 – for the left side of pins (PIN 2, 3, 4, 5, 6) and R0/R1/R2 - for the right side (PIN 8, 9, 10, 11, 12). All the patterns have inter-independent settings and can be used by a random quantity of Clock generators connected up to the pins on the corresponding side. Connections configuration is indicated in the generator's name, connected to pin. For instance, a Clock generator which is connected to pin 2 and L0 pattern will have a CL0 index (Clock, Left, Pattern number 0).

Configuration Options:

Pattern number:	Pattern L0/L1/L2/R0/R1/R2	- connect to pattern
Frequency:		- generator frequency
Duty cycle:	In percent	- duration of high signal in percentage

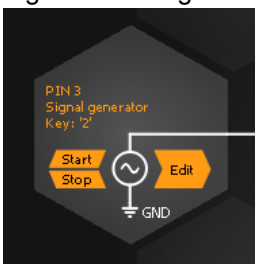
Figure 8-23. Clock Generator View



'Start' and 'Stop' buttons can be used to start and stop a current generator. A 'Pause' button used for generator pause/start at the same time makes the Clock generator key connect/disconnect. If 'All' flag is enabled, the buttons do the same as buttons in the emulator.

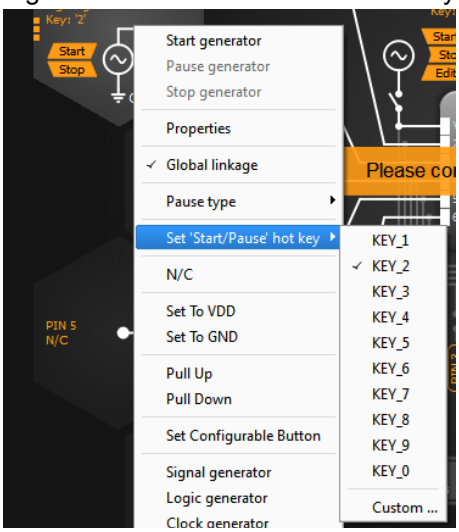
8.2.5. Signal (Analog) Generator

Figure 8-24. Signal Generator



Signal generator is used to generate analog signals: Constant Voltage level, Sine, Trapeze(Trapezoid), User defined.
Logic, signal and clock generators can be started/paused/stopped using orange buttons or through the context menu. The user can also assign the hot keys for start/pause.
Several generators can use the same hot button to start/pause at once. This is how to start more than one generator at the same time.

Figure 8-25. Sets Start/Pause Hot Key



Signal Generator Settings

Type: Const voltage level/Sine/User Defined - type of waveform;

Constant Value:

U: - voltage level;

Figure 8-26. Constant Value

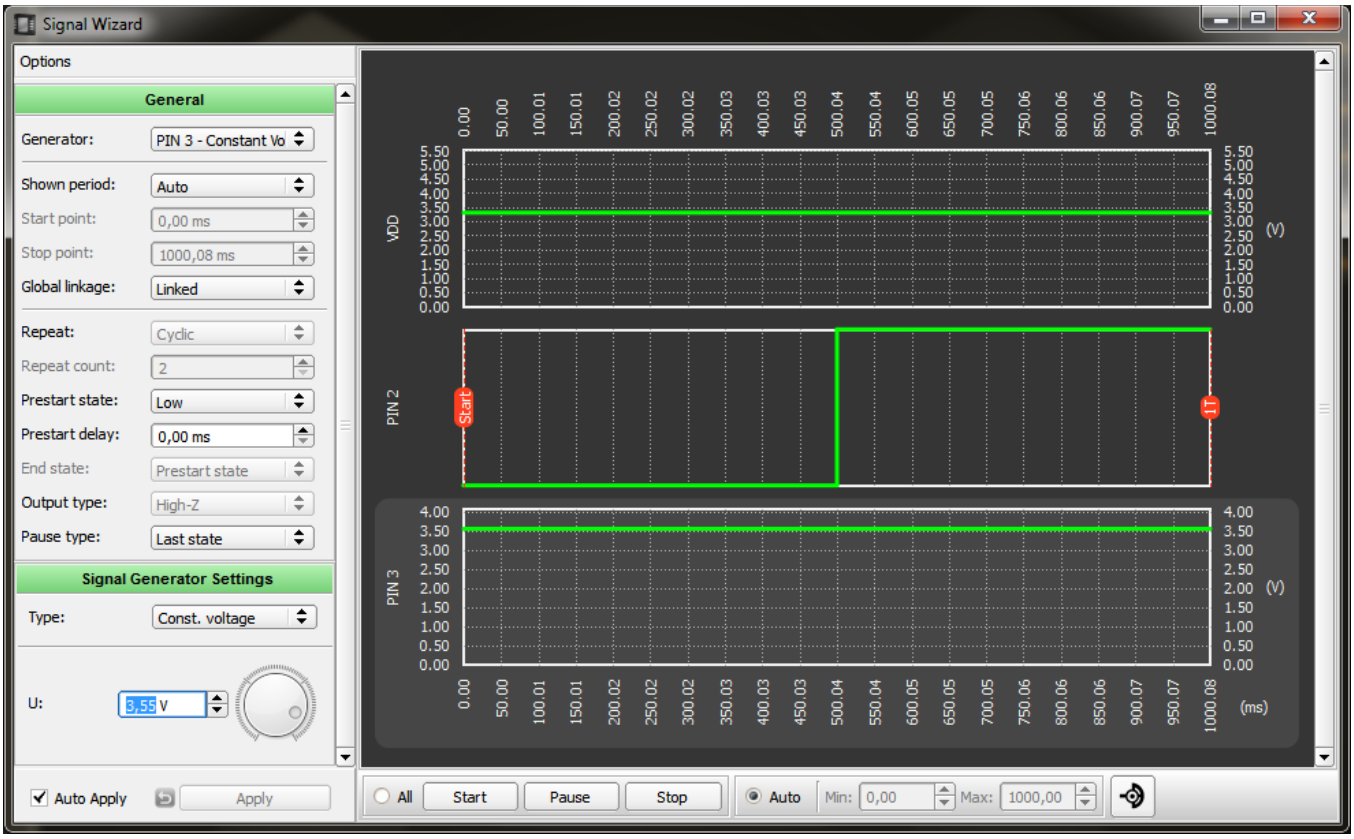
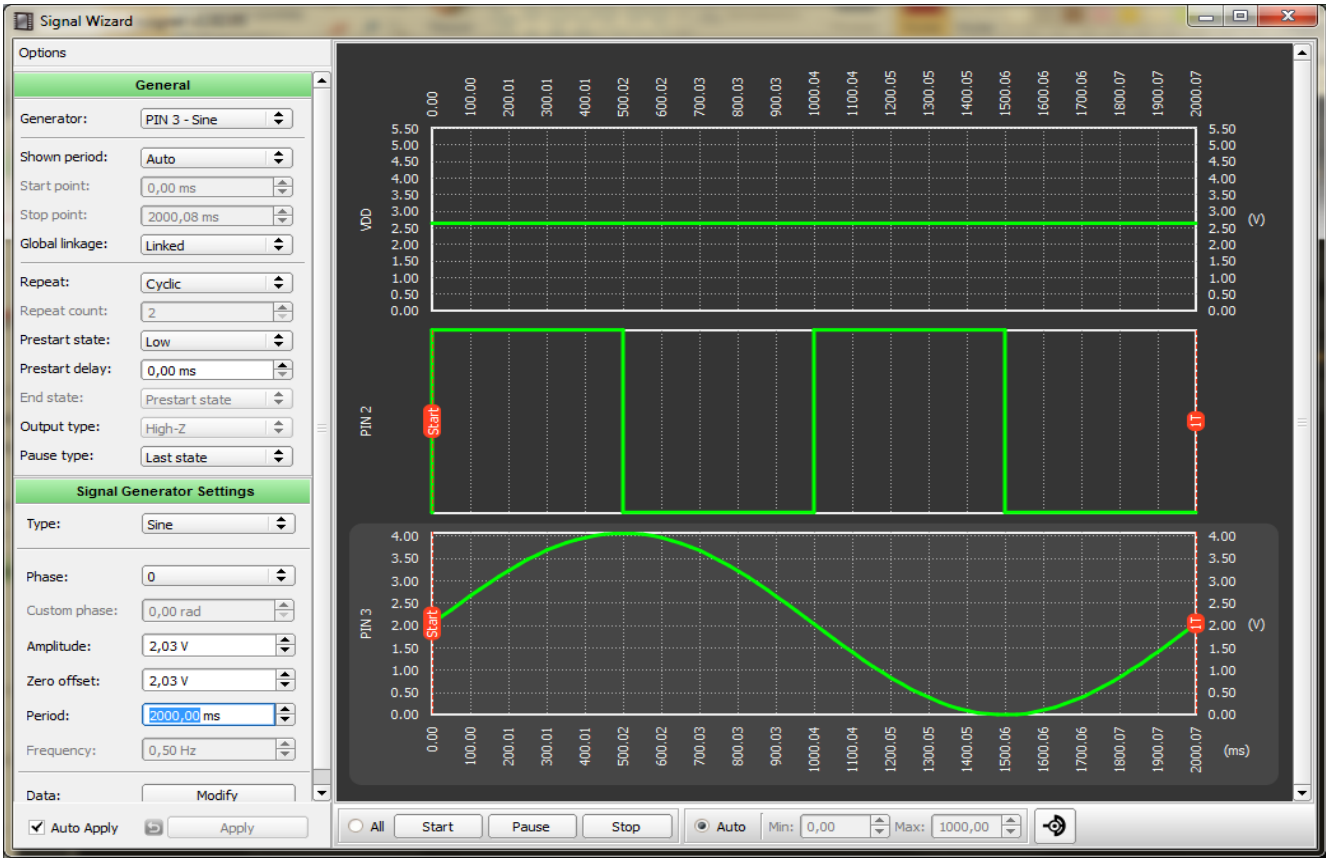


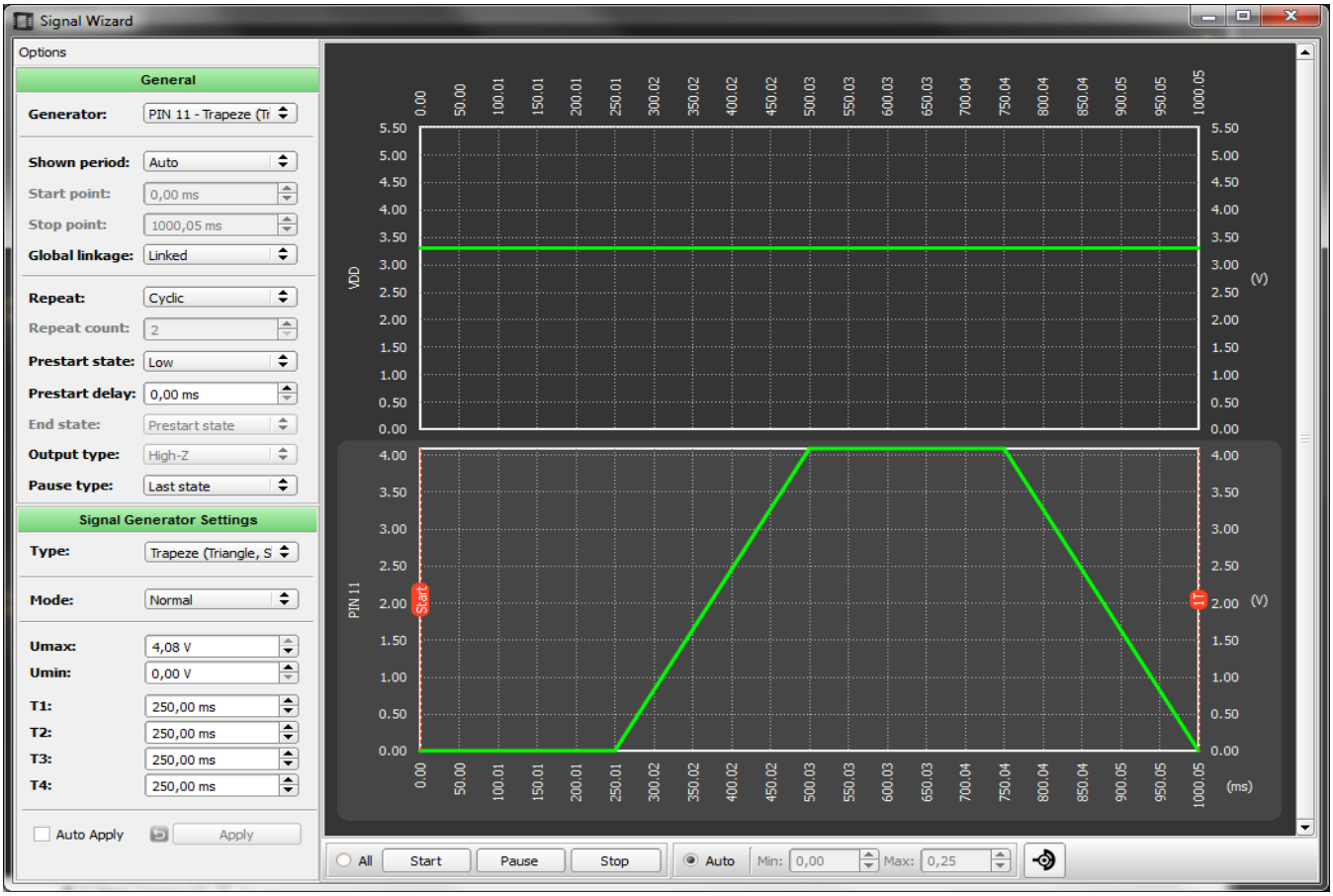
Figure 8-27. Sine



Sine Settings:

Repeat:	One shot/Cyclic/Custom	- repeat option
Phase:	Custom/0/Pi:2/Pi/3Pi:2	- φ0
Custom phase:		- show phase in a radian
Amplitude:		- amplitude
Zero offset:		- zero offset
Period:		- period
Frequency:		- shows frequency
Data:		- change signal using Custom Signal Wizard

Figure 8-28. Trapezoid (Triangle, Saw)



Trapeze Settings:

Mode:	Normal/Invert	-signal mode
Umax/Umin		-max/min voltage level
T1, T2, T3, T4		-duration of trapeze

If T_3 = 1 signal is a triangle.
If T_3 = 1, T_2 = 2 or T_4 = 2 signal is a sawtooth.

Figure 8-29. Duration of Trapeze (Trapezoid)

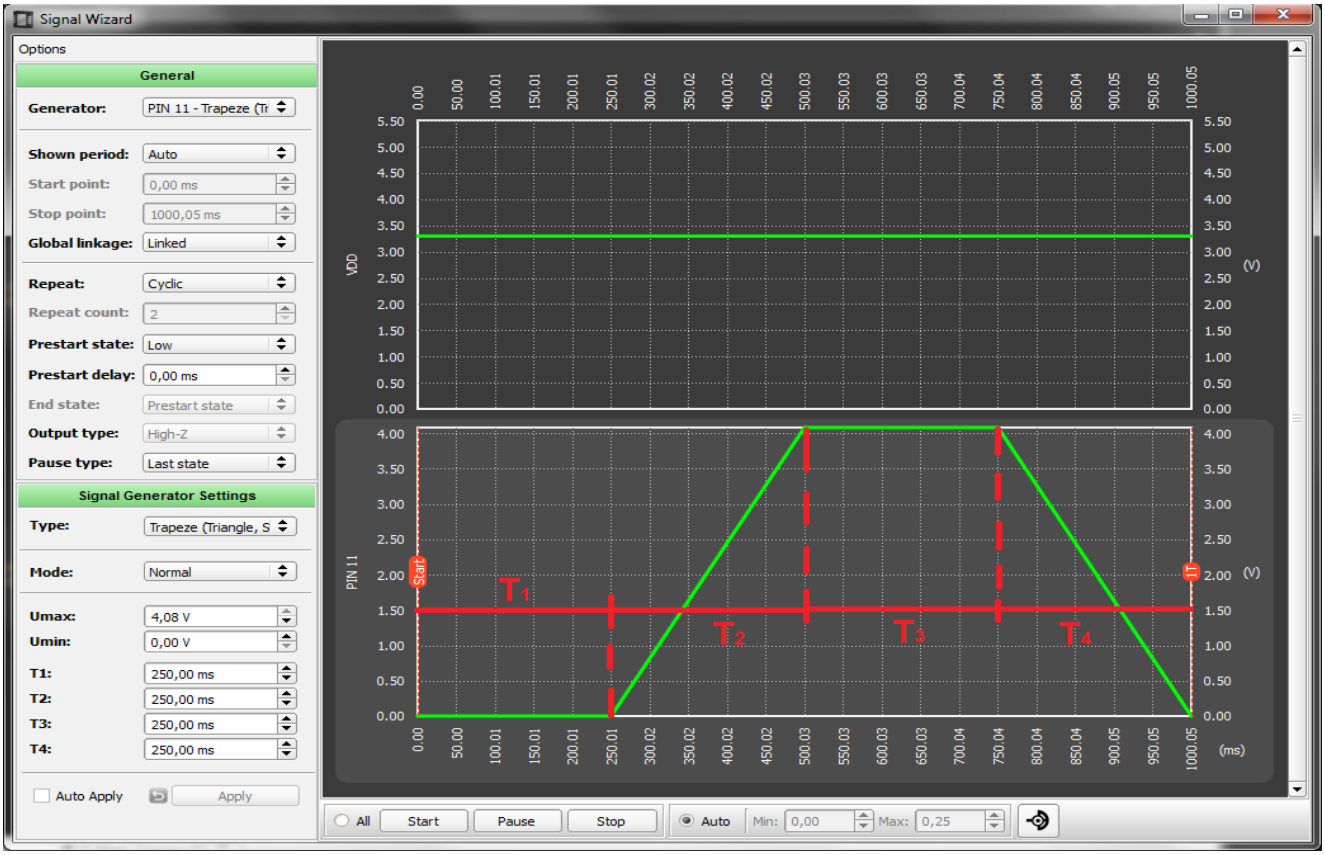
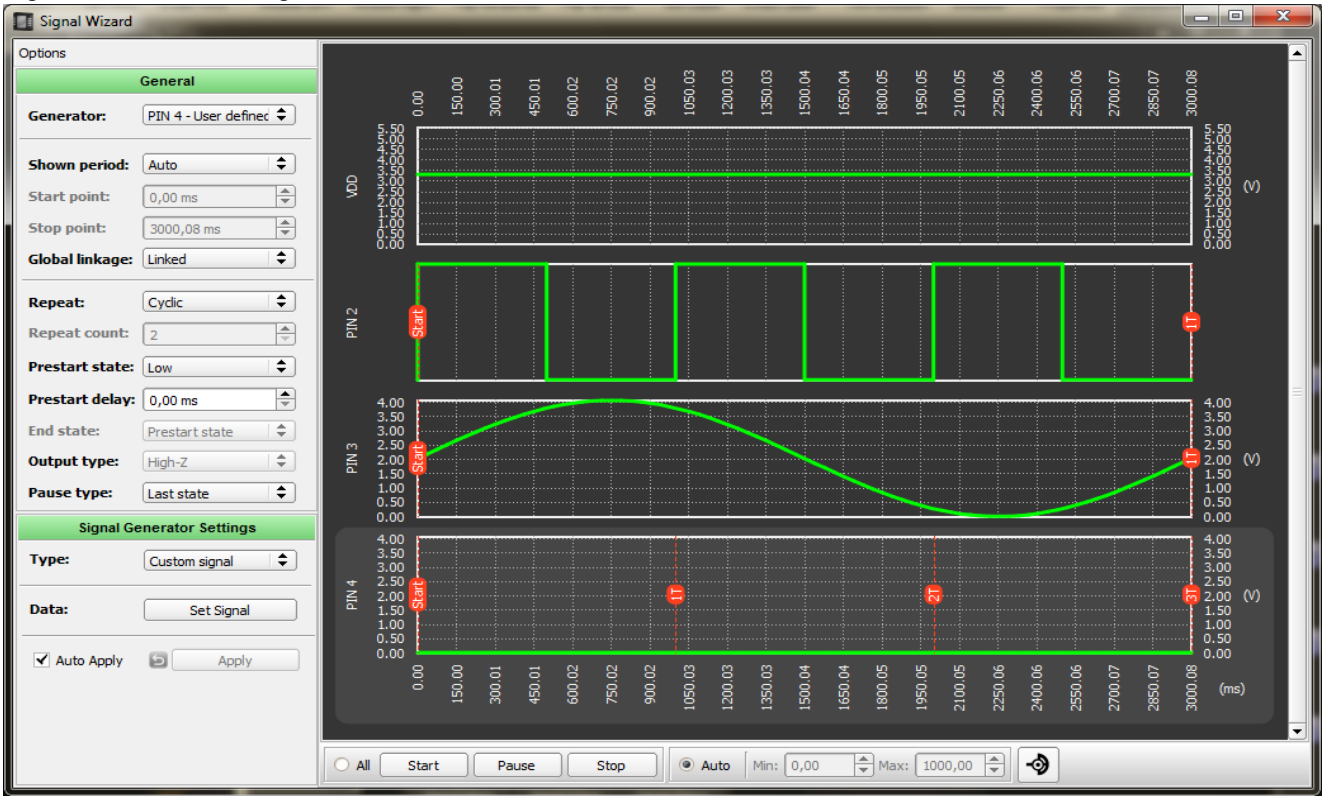


Figure 8-30. Custom Signal

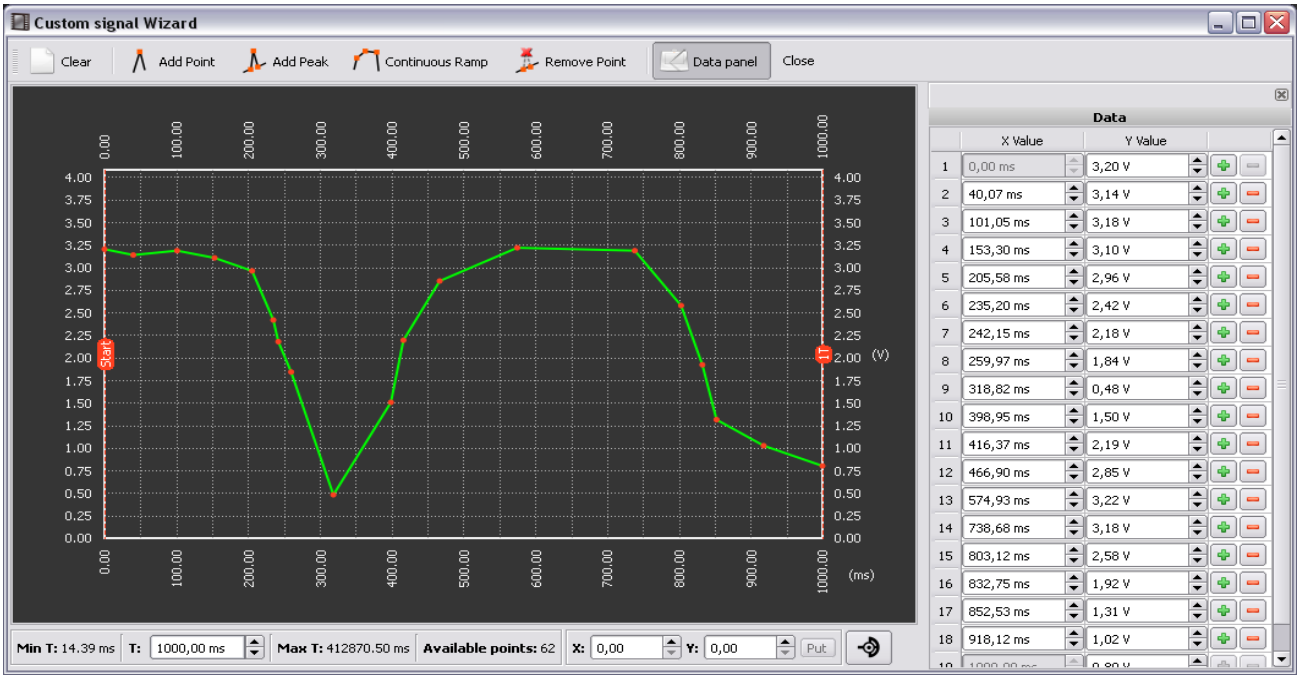


Custom Signal Settings:

Repeat:	One shot/Cyclic/Custom	- repeat option;
Data:	Set Signal	- change signal using Custom Signal Wizard

8.2.6. Custom Signal Wizard

Figure 8-31. Drawing Signal (Arbitrary waveform)



Toolbar:	Clear	- clear data
	Add Point/Add Peak/Continuous Ramp/Remove Point	- draw mode
	Data panel	- turn on/off the data table
	Close	- close window with current signal

Figure 8-32. Peak

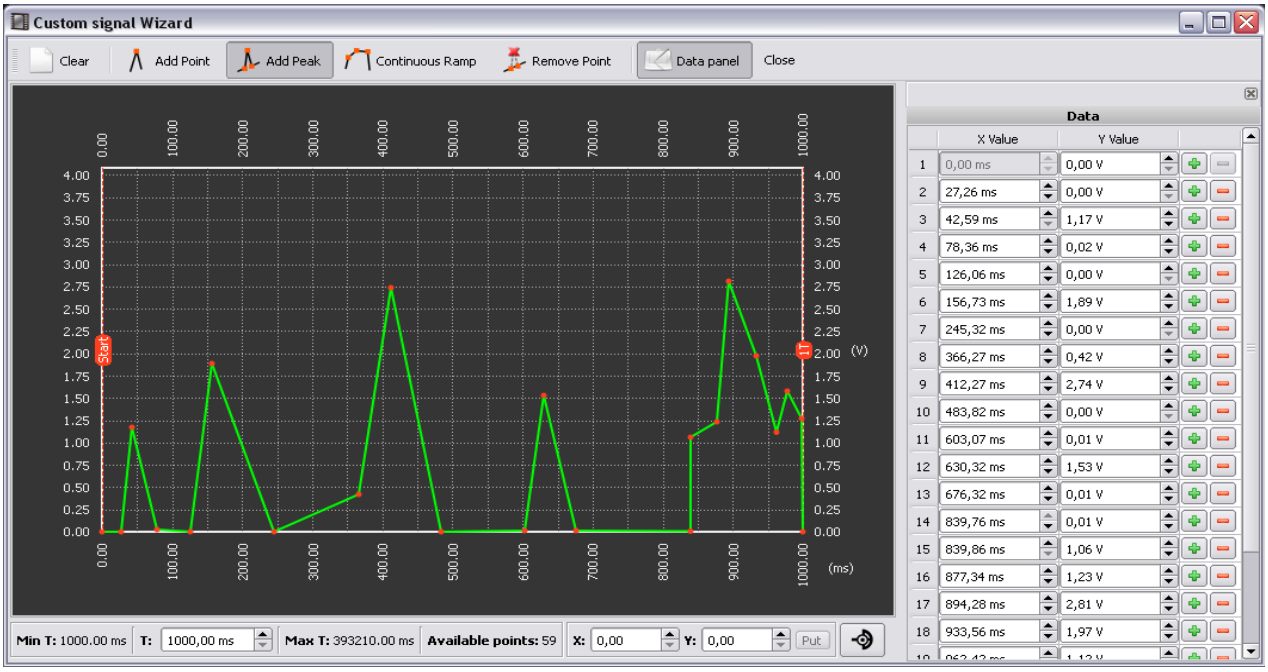
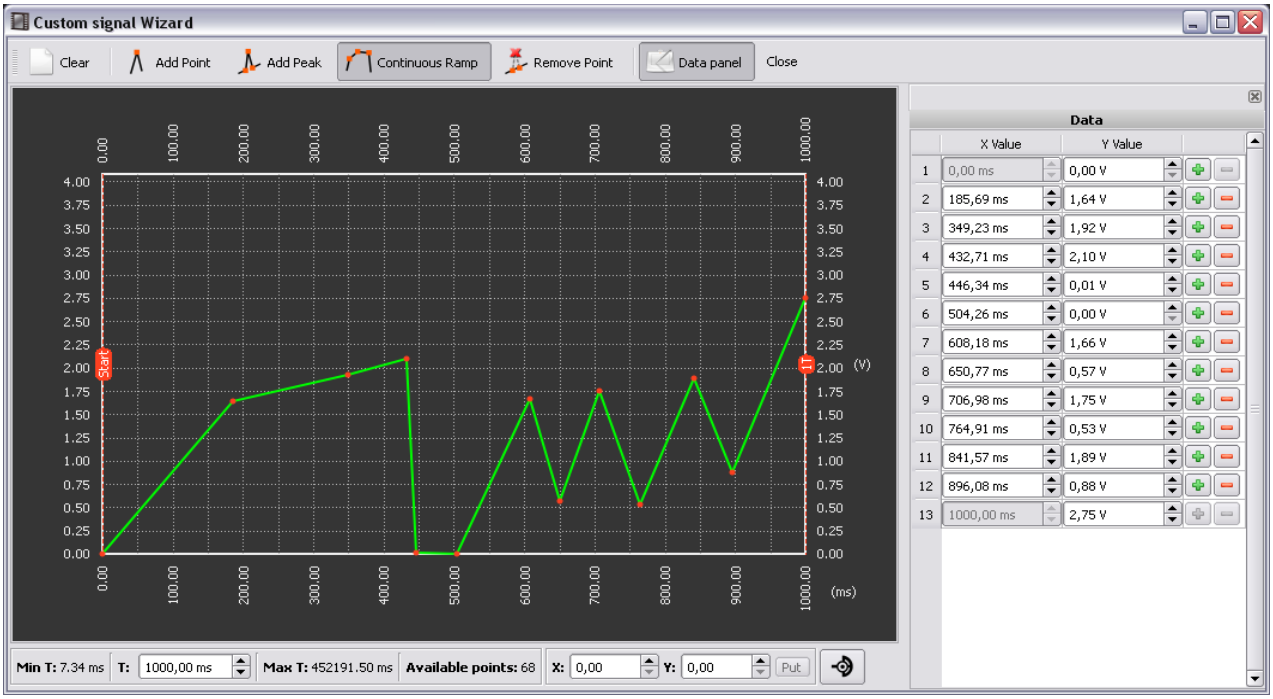


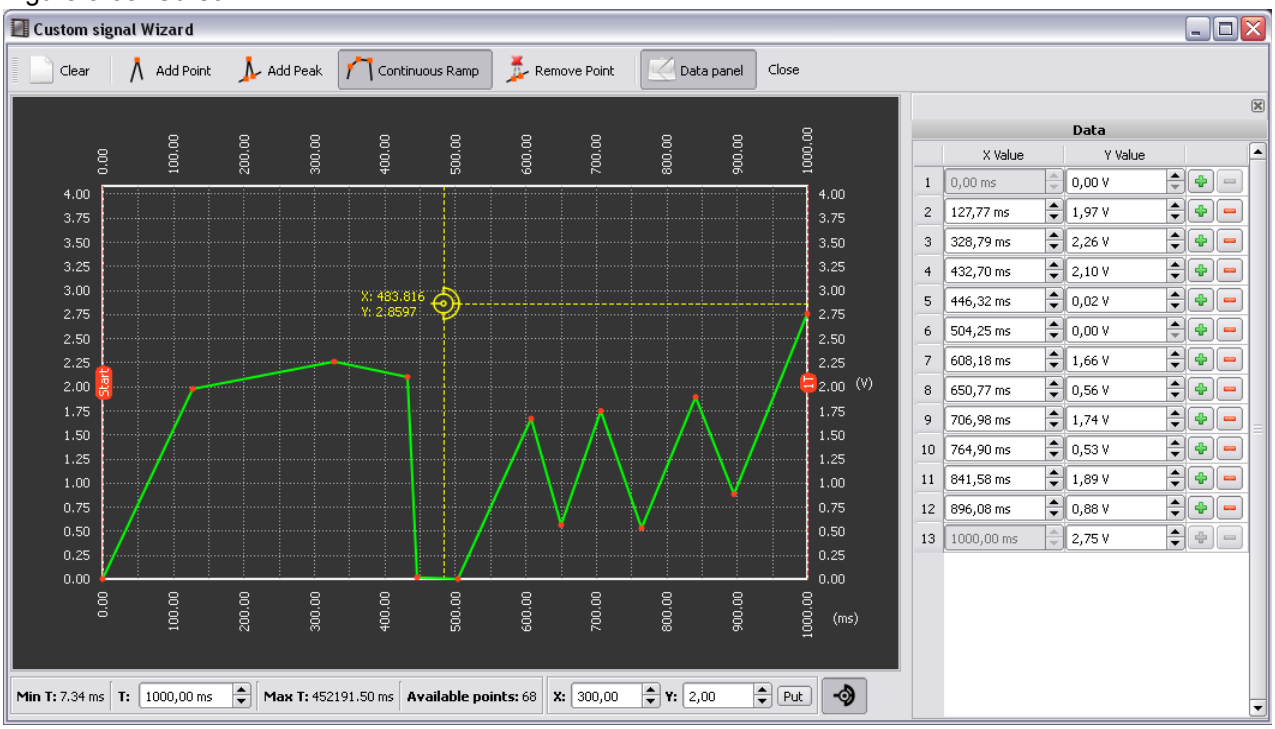
Figure 8-33. Continuous Ramp



Remove Point: Removes selected point. Double clicking on the point can also remove it.

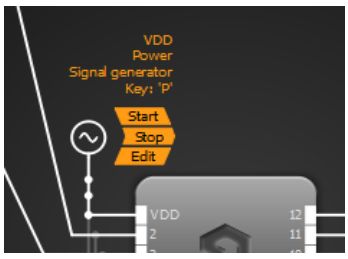
Figure 8-34. Data Panel

Figure 8-35. Cursor



8.2.7. VDD Power Signal Generator

Figure 8-36. VDD Power Signal Generator

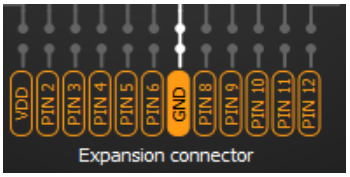


Simple signal generator for VDD with its own options.

8.3. Expansion Connector

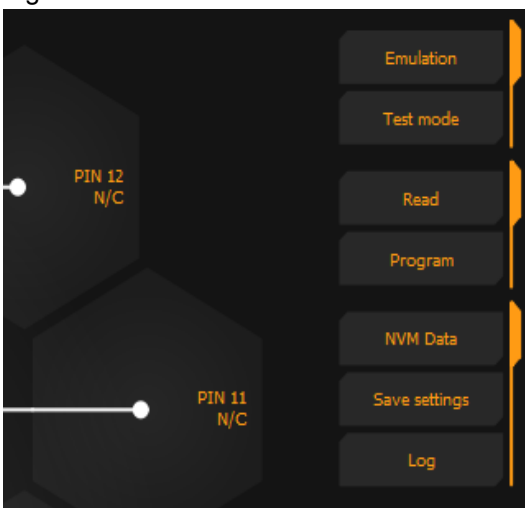
User can connect/disconnect I/O pads of GreenPAK with the expansion connector on the board.

Figure 8-37. Expansion Connector



8.4. Control Panel

Figure 8-38. Control Panel

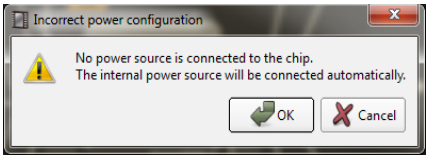


Emulation:

The current project will be loaded to the chip (but not programmed), and will be ready for the test on the emulation board. The user can also change any configuration during the emulation process.

In case when Power key and VDD key on the Expansion connector are turned off there will pop up a warning message (figure 8-39).

Figure 8-39. Incorrect Power Configuration


Incorrect power configuration
No power source is connected to the chip.
The internal power source will be connected automatically.
OK
Cancel

Test Mode:

The test mode is used to connect or disconnect chip's I/O pads to stimulus areas, configured by the user.
The user can also check the programmed chip using the test mode without emulation. In order to do this one only needs to turn on the test mode and power key. The test mode can work without power on the chip. User will control the Power key manually.

Read:

Read chip using emulation board.

Program:

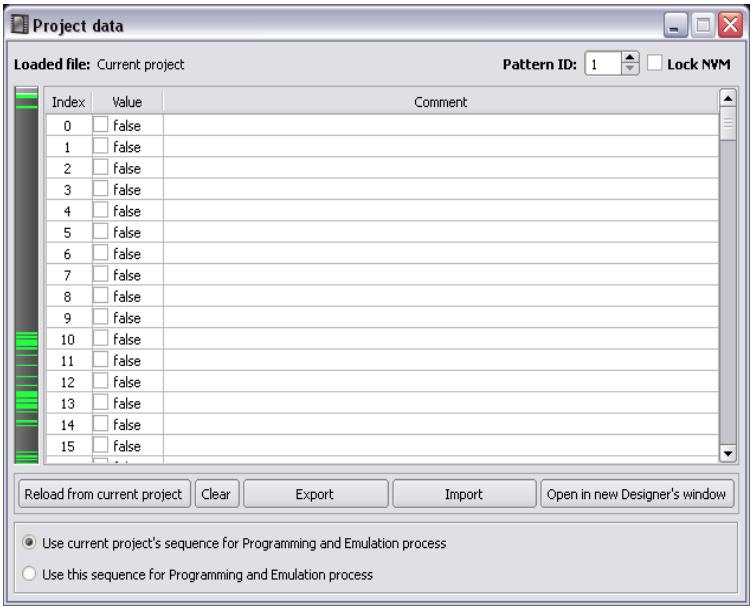
Program chip with the current project.

NVM Data:

The table of bits.
Pattern ID – gives an ID (1-255) to the project. The ID will be put into the chip after programming, and also will be read during "chip reading" operation.
Lock NVM – blocks NVM reading. A programmed project becomes unavailable for chip reading. However, the chip is still available for emulation.

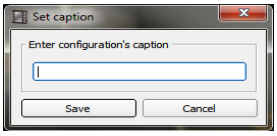
Use current project's sequence for Programming end Emulation process – user can choose to use current project's sequence for programing and emulation process.
Use this sequence for Programming end Emulation process – user can choose current sequence for programming and emulation process.
Reload from current project – user can load bit sequence from current project.
Clear – sets all bits in false.
Export – save data to text file.
Import – load data from text file.
Open in new Designer's window – open current bit sequence in new Designer's window.

Figure 8-40. NVM Data



Save Settings:
Save current configuration of a test mode to the project file.

Figure 8-41. Save Project



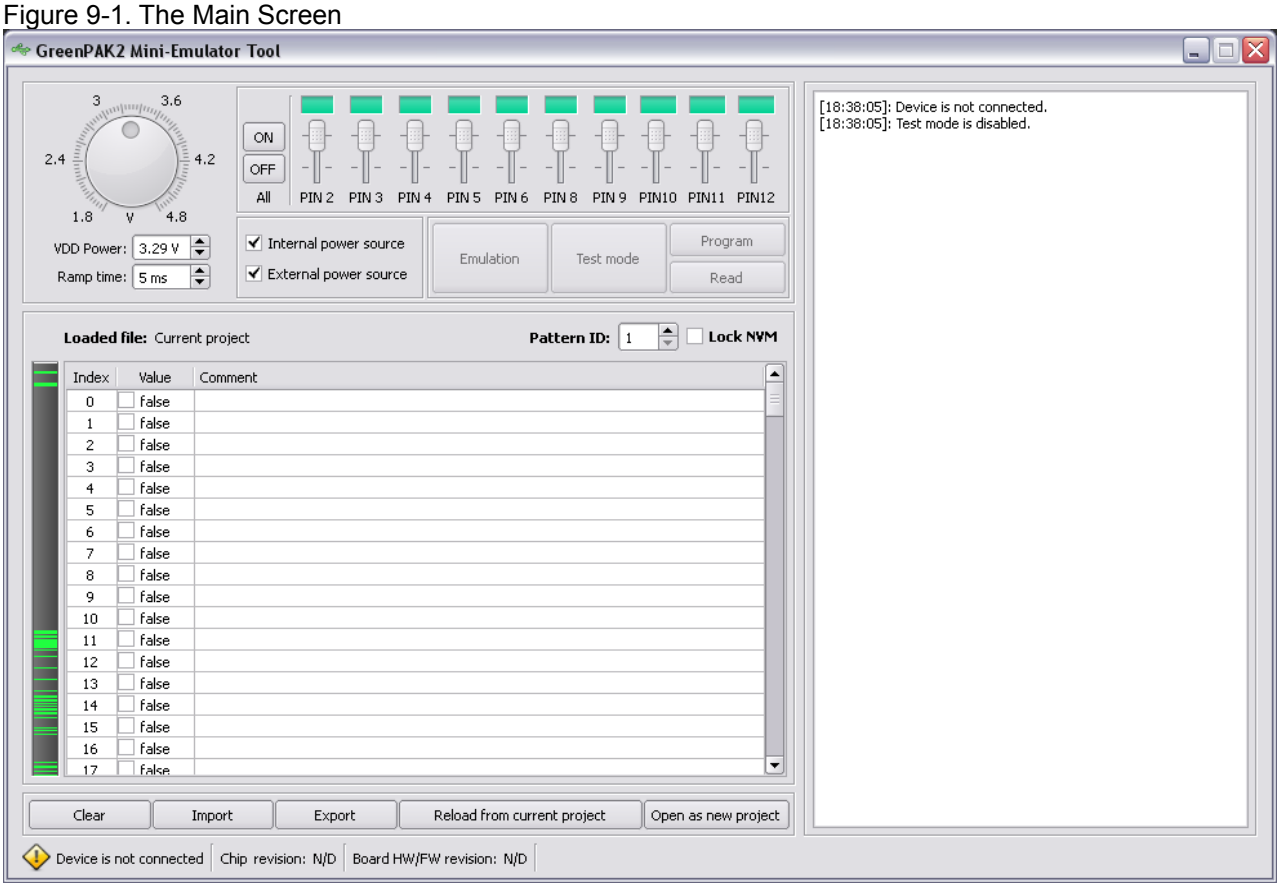
Log:
Show log.

Figure 8-42. Test Mode Configuration

User can save current configuration of a test mode to the project file (Figure 8-42).

9. GreenPAK 2 Mini-Emulation Board

Figure 9-1. The Main Screen



VDD Power – defines the voltage level, set on the GreenPAK (Internal power source) when the 'Test mode' is ON.

Ramp time – time of voltage increases from 0 V to the level specified in the VDD Power while turning the 'Test mode' ON.

Pattern ID – gives an ID (1-255) to the project. The ID will be put in the chip after programming, and also will be read while chip reading.

Lock NVM – blocks NVM reading. A programmed project becomes unavailable for chip reading. The chip is still available for emulation.

User can connect/disconnect I/O pads of GreenPAK 2 with the expansion connector on the board using PIN2, PIN3, PIN4, …latches.

The ‘Test mode’ button is used for turning on/off the test mode.

The 'Emulation' button turns on/off the Emulation mode.
In Emulation mode, the Test mode will be automatically turned on. Thus the current project will be loaded to the chip (but not programmed), and will be ready for test on the emulation board. The user can change any configuration during the emulation process.
The user can also check the programmed chip using test mode without emulation. In order to do this one only needs to turn on the test mode and power key.

A 'Program' button is used for writing NVM to chip.

A 'Read' button is used for reading NVM from chip.

A 'Clear' button resets all values to “false”.

'Export'/'Import' buttons are used for saving/opening NVM in *.txt format.

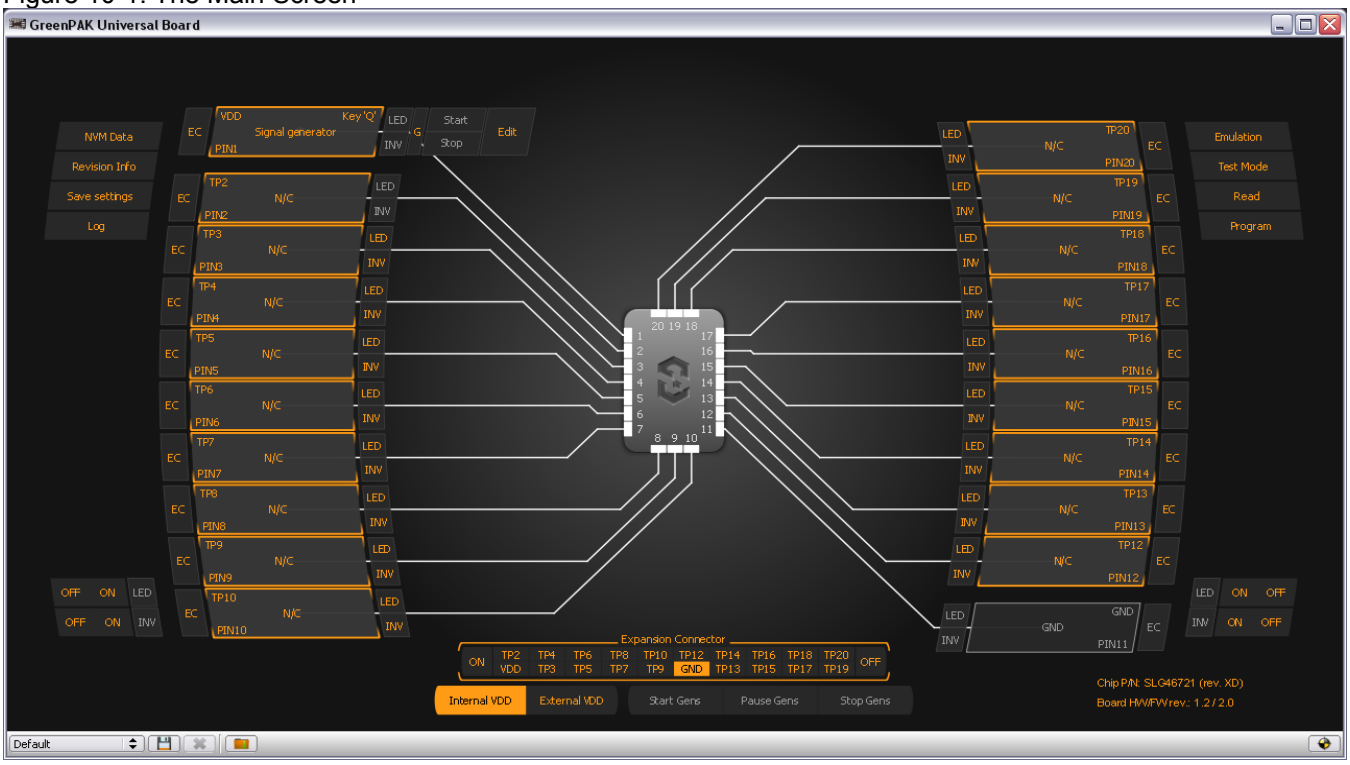
'Reload from current project' – updates NVM from current project.

'Open as a new project' – creates a new project in GreenPAK Designer with current NVM configuration.

Below the mini-emulator window, there is the information about device, chip revision, and board hardware/freeware revision.

10. GreenPAK 3-4 Emulation Board

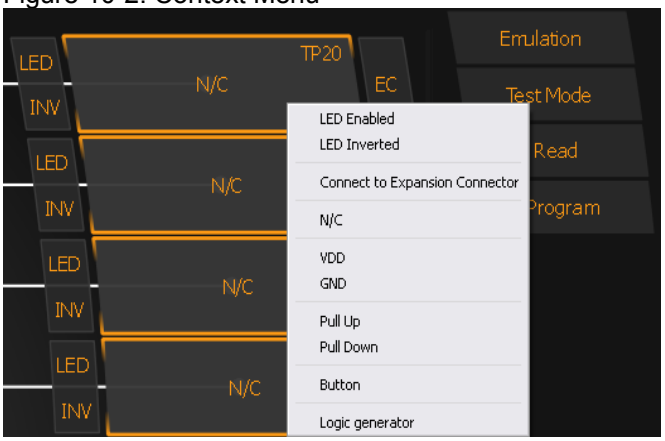
Figure 10-1. The Main Screen



In figure 10-1 one can see the GreenPAK IC with stimulus areas and expansion connectors which are connected to pins. There are 2 panels with buttons in the top left and top right corners, which provide the emulation process.

Stimulus Areas are used to configure input connections. Use the context menu to manage them.

Figure 10-2. Context Menu



10.1. Types of Areas

Fixed Inputs (Figure 10-3 – 10-7).

Figure 10-3. N/C (not connected)

Figure 10-4. Set to VDD

Figure 10-5. Set to GND

Figure 10-6. Pull Up

Figure 10-7. Pull Down

LED's (Figure 10-8, 10-9)

Figure 10-8. Inverted Buffered LED, Inverted Buffered LED+Pull Up, Inverted Buffered LED+Pull Down

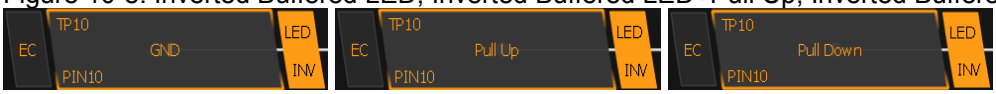
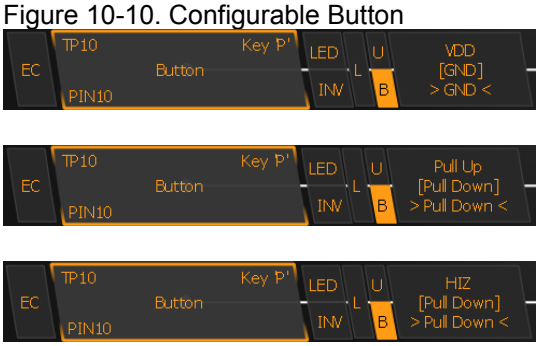


Figure 10-9. Buffered LED, Buffered LED+Pull Up, Buffered LED+Pull Down

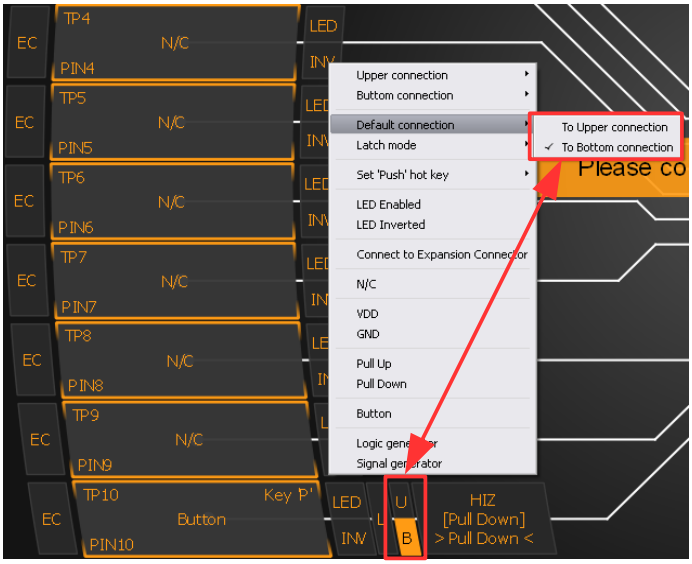
Configurable Input (Figure 10-10)

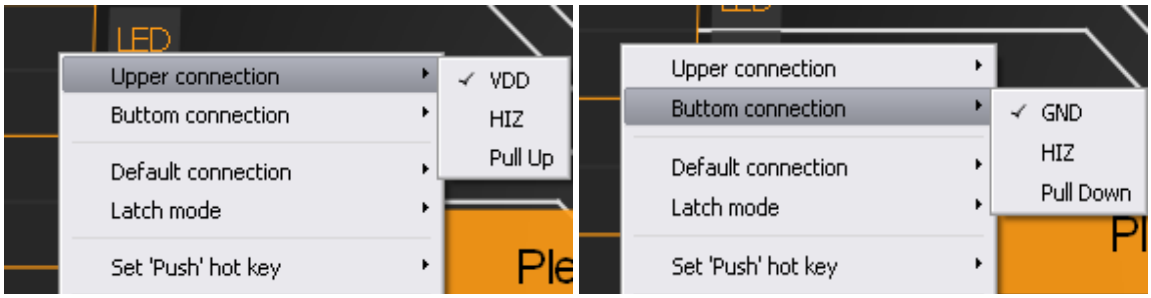
Figure 10-10. Configurable Button



The default connection can be set to either Upper connection or Bottom connection. Click your mouse over the key U or B to change the value.
The user can configure each connection to VDD/GND, High-Z or Pull Up/Down.

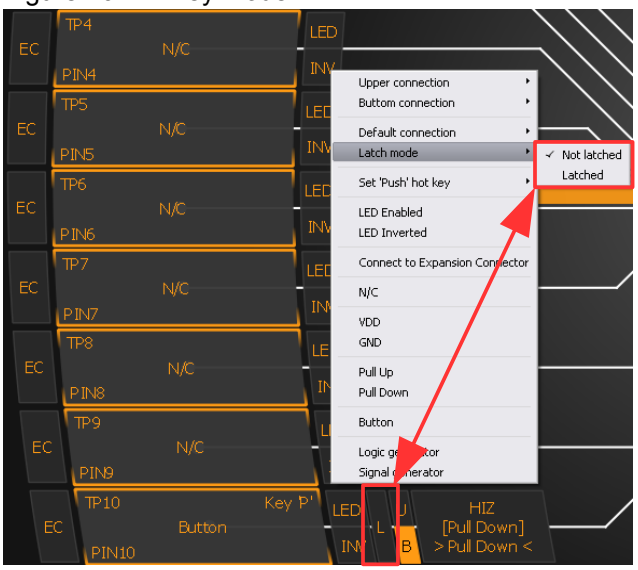
Figure 10-11. Default Key Connection





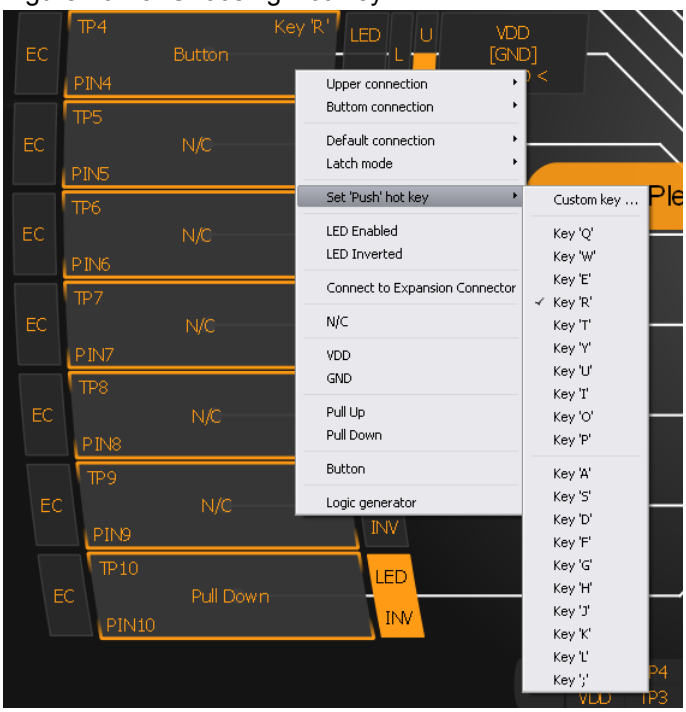
The switch has 2 modes: Latched, Unlatched which can be configured from the context menu or click your mouse over the key L to change the value.

Figure 10-12. Key Mode



User can assign Hot Key for 'Push' action. The assigned key will simulate mouse click over the key:

Figure 10-13. Choosing Hot Key

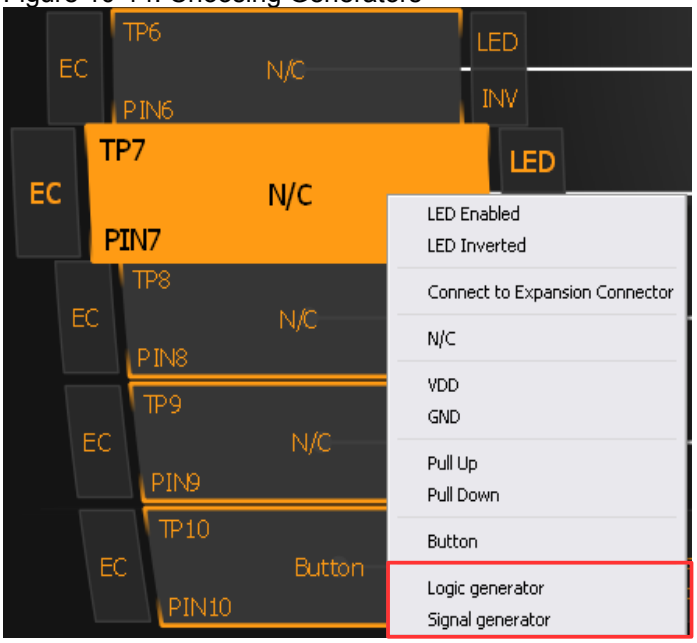


User can assign the same hot key to other Switches which allows changing the key values of all the Switches with the same hot key at once.

10.2. Generators

To each chip there can be connected 2 types of generators: Logic generator or Signal generator.

Figure 10-14. Choosing Generators



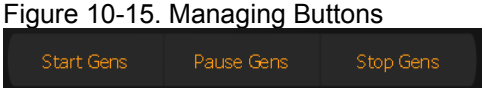
Each generator has its own settings. For the settings window to appear press the Edit button.

On the left, you can see the options table divided into 2 groups:

1. General – applied to all types of generators
2. Special for each generator

For them to start up, use the buttons below the Emulator.

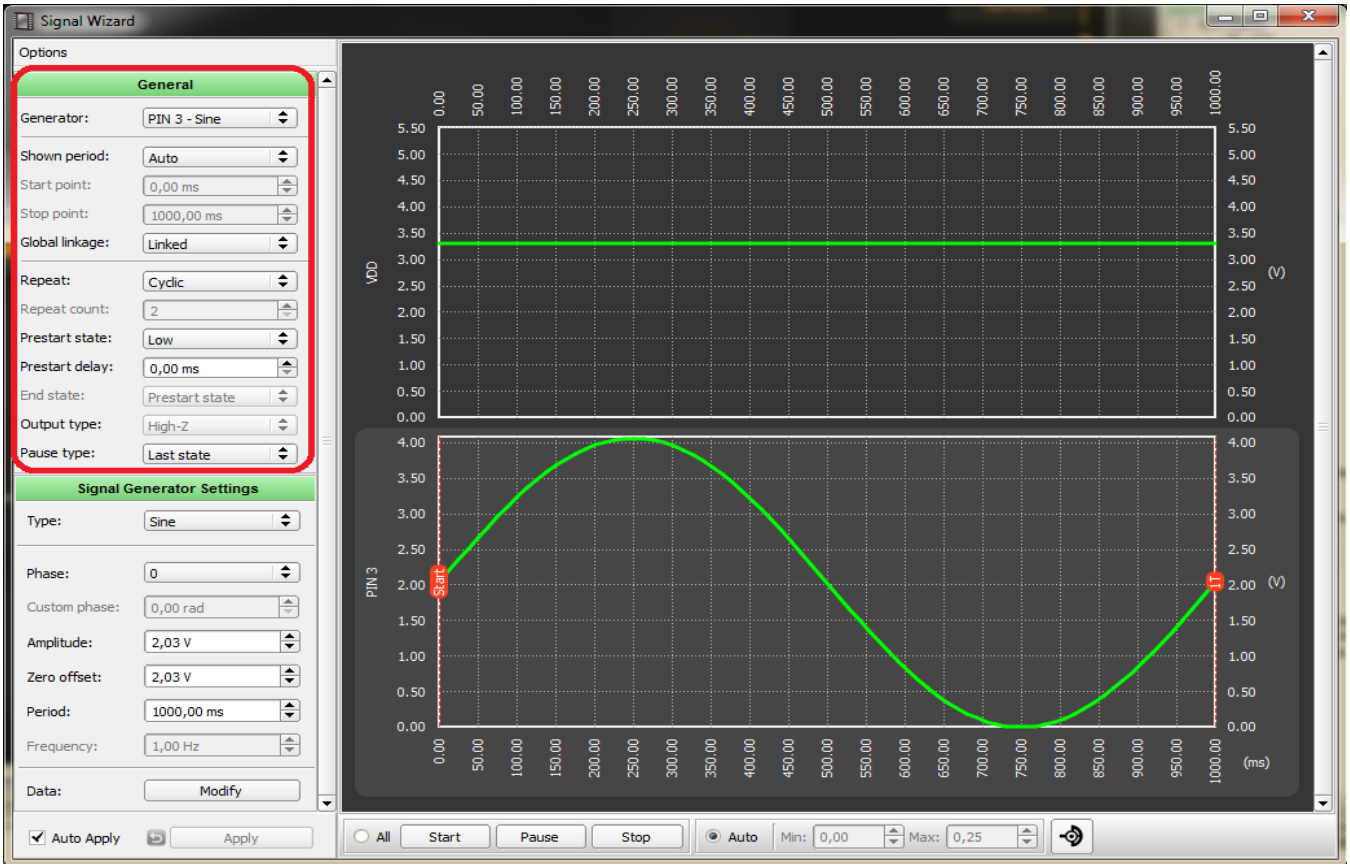
Figure 10-15. Managing Buttons



Note: these buttons can be controlled only by generators with an installed Global Linkage flag

10.2.1. General Options in a Signal Wizard Mode

Figure 10-16. General Option



Generator:		- generator selector
Shown period:	Auto/Custom/1T/2T/3T/4T	- set the period of a current generator to be displayed
Global linkage	Linked/Unlinked	-if generator is linked, it will be controlled by buttons “Start”, “Stop” and “Pause” on the Emulator
Repeat	One shot/Cyclic/Custom	- repeat option
Prestart state	Low/Start point(V0)/High-Z	-state before start
Prestart delay		-delay before start
End state	Keep last state/Prestart state	-pin state after generation
Output type	High-Z/Strong Drive/Open Drain, Drives High/ Open Drain, Drives Low/Resistive Pull Up/ Resistive Pull Down/ Resistive Pull Up/Down	- type of output
Pause type	Last state/Low/High/High-Z	-state when it is paused

10.2.2. Period Modes

AUTO Mode

All generators with 'AUTO' option have one scale; this scale = MAX period of all generators with 'AUTO' option.

Figure 10-17. One Scale for All Generators

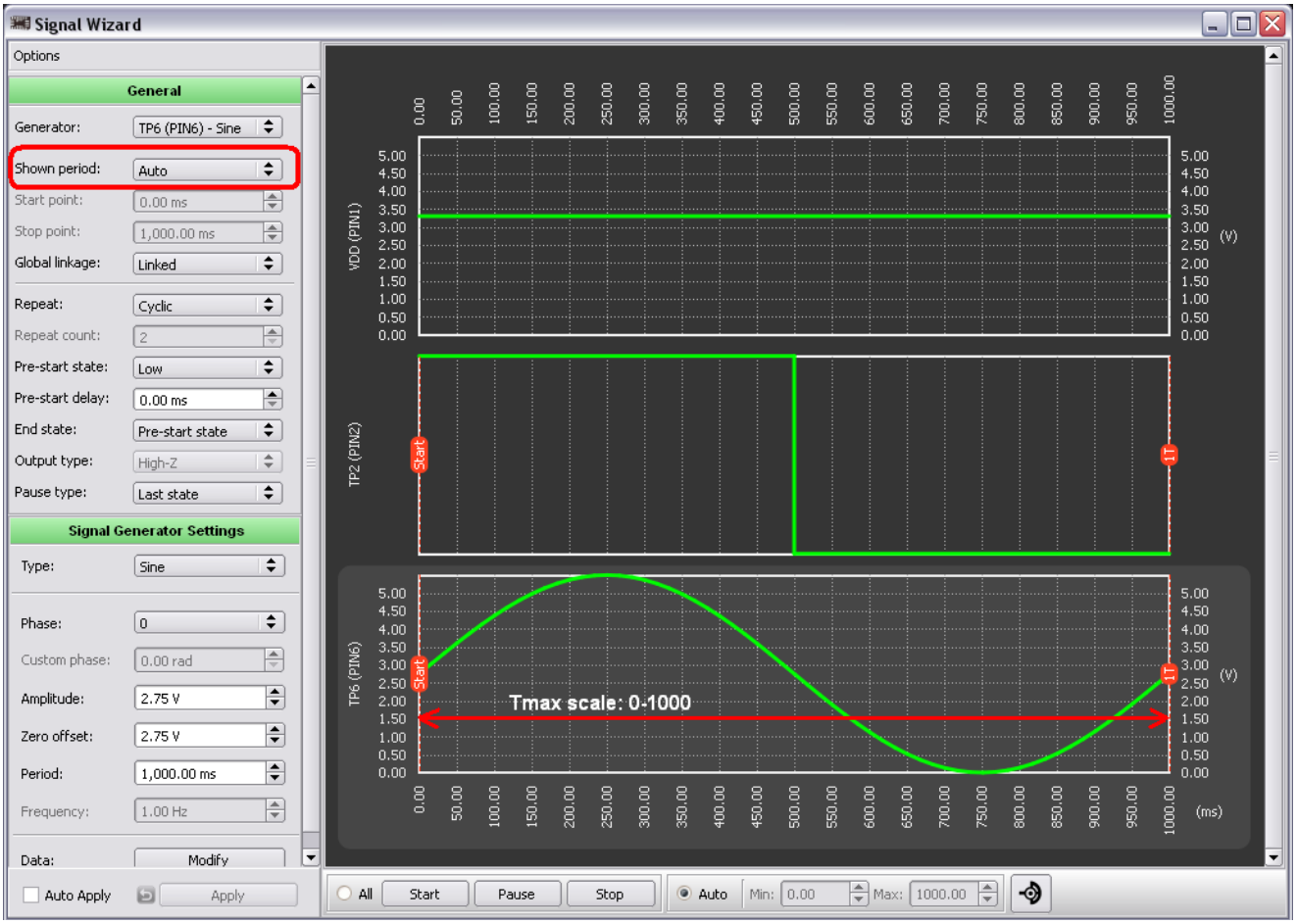
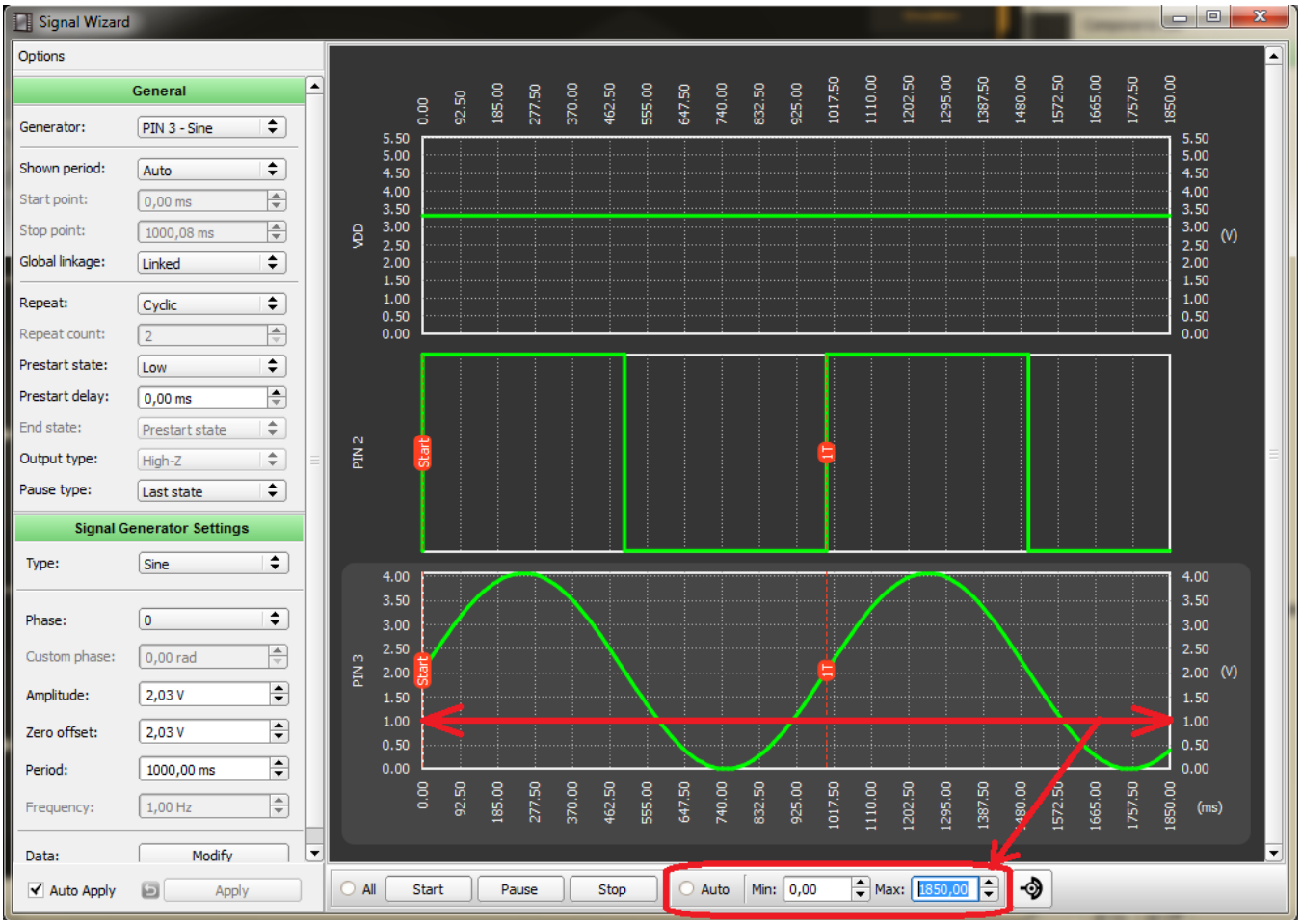


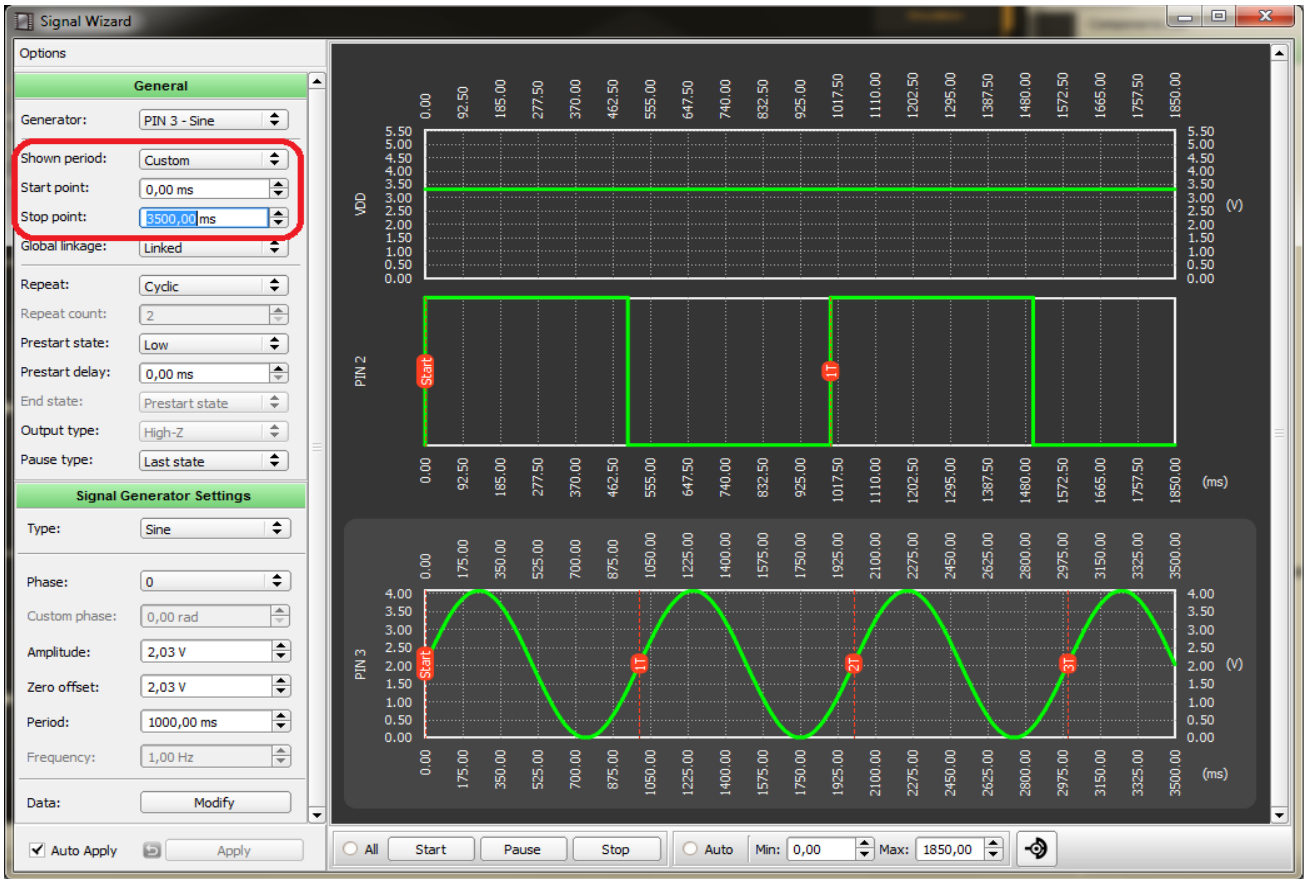
Figure 10-18. User Can Change the Scale Manually



button turns on/off the mouse coordinates in the timing diagrams.

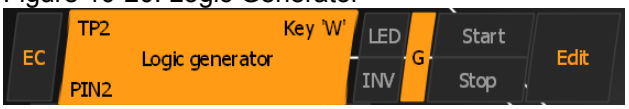
CUSTOM Mode

Figure 10-19. Choosing Period Options



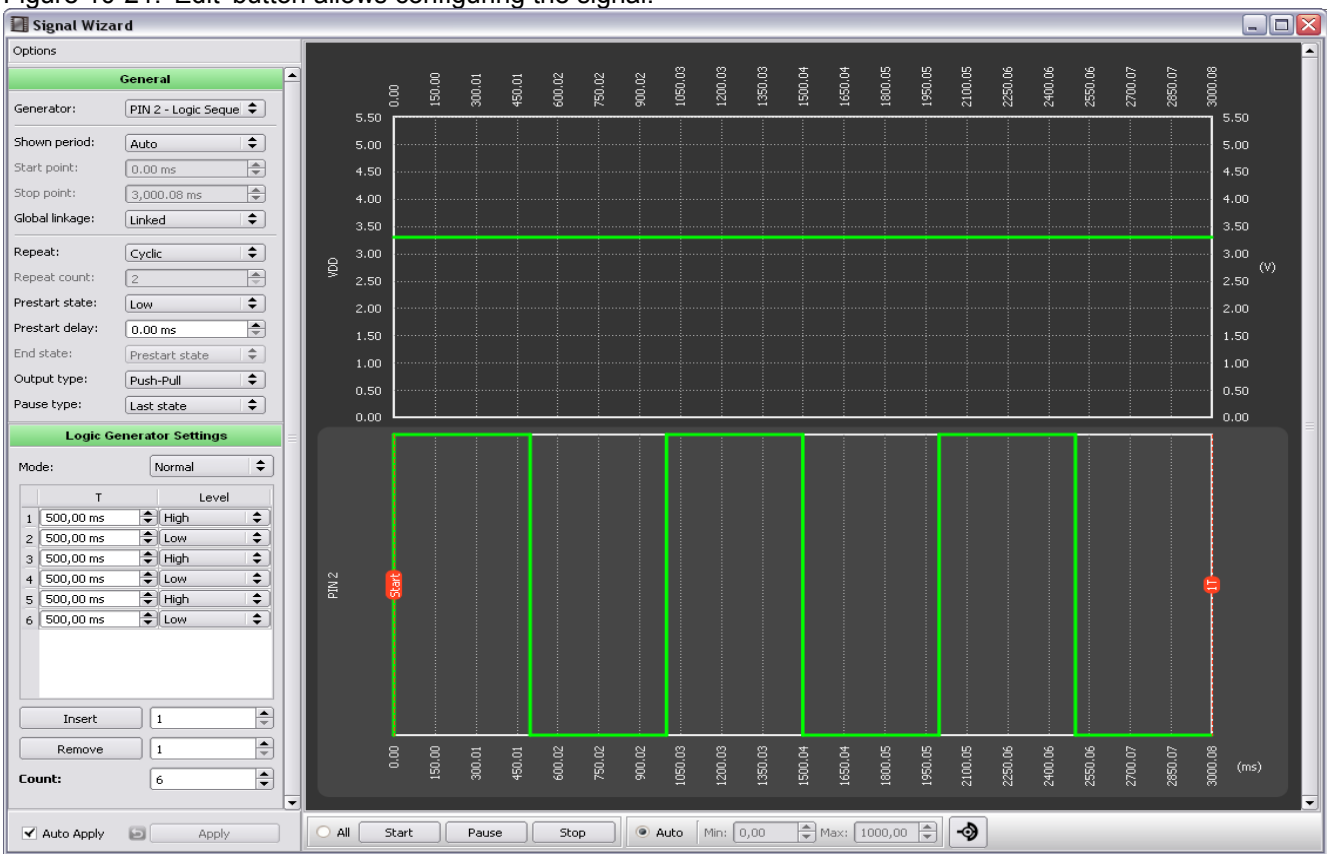
10.2.3. Logic Generator

Figure 10-20. Logic Generator



Logic generator is used for generating the logic pulses.

Figure 10-21. 'Edit' button allows configuring the signal.

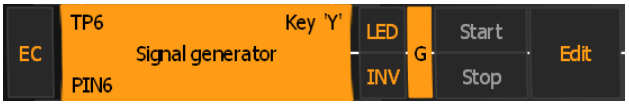


Configuration options:

Mode:	Normal/Invert	- signal mode
Repeat:	One shot/Cyclic/Custom	- repeat option
T/Level:		- sets duration of level
Insert:		- insert pulse to the entered position;
Remove:		- remove pulse from the entered position;
Count:		- pulse count

10.2.4. Signal (Analog) Generator

Figure 10-22. Signal Generator



Signal generator is used to generate analog signals: Constant Voltage level, Sine, Trapeze(Trapezoid), Logic pattern and User-defined.

Logic and signal generators can be started/paused/stopped using orange buttons or through the context menu. The user can also assign the hot keys for start/pause.

More than one generator can use the same hot button to start/pause at once. This is how to start more than one generator at the same time.

Figure 10-23. Sets Start/Pause Hot Key

Signal Generator Settings

Type: Const voltage level/Trapeze/Logic pattern/Sine/Custom - type of waveform;

Constant value:

U: - voltage level;

Figure 10-24. Constant Value

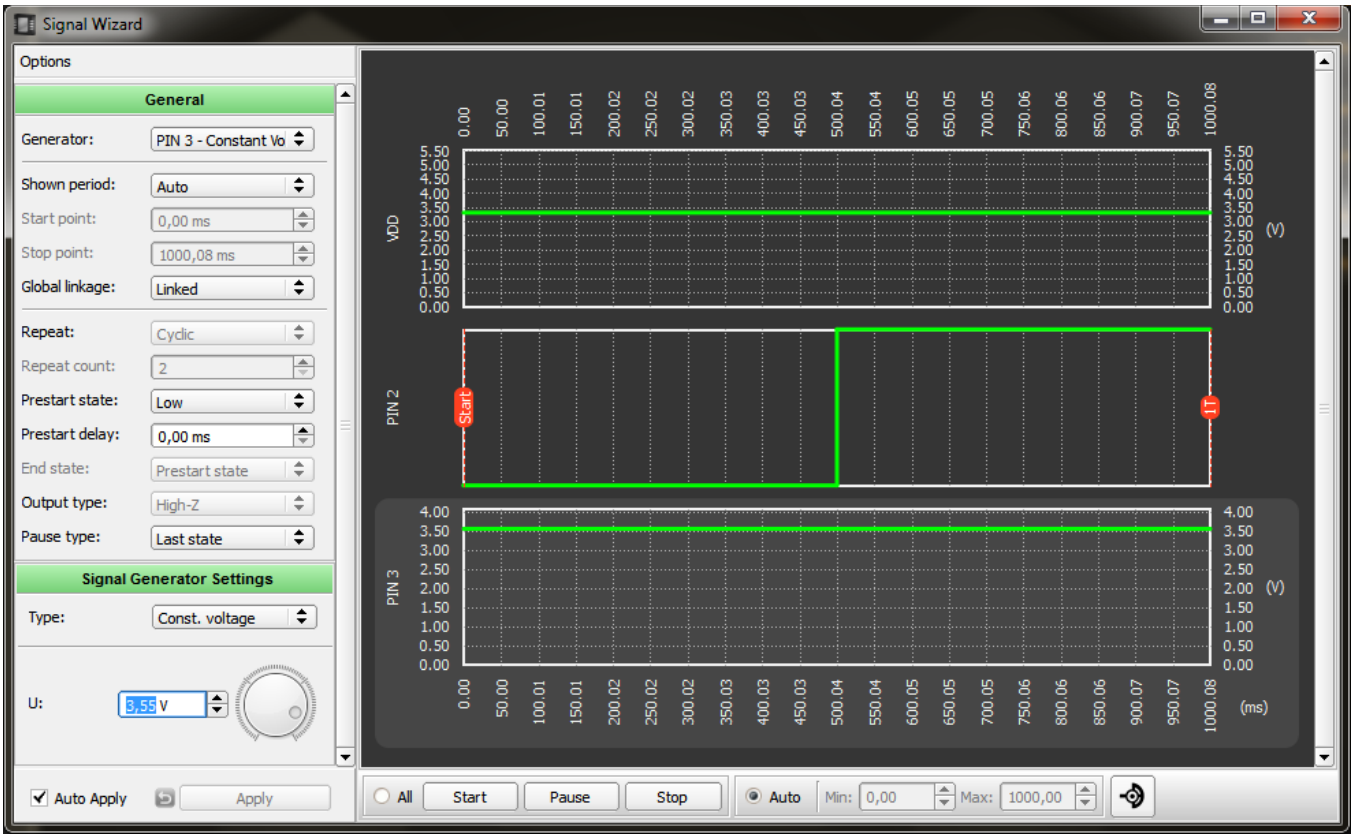
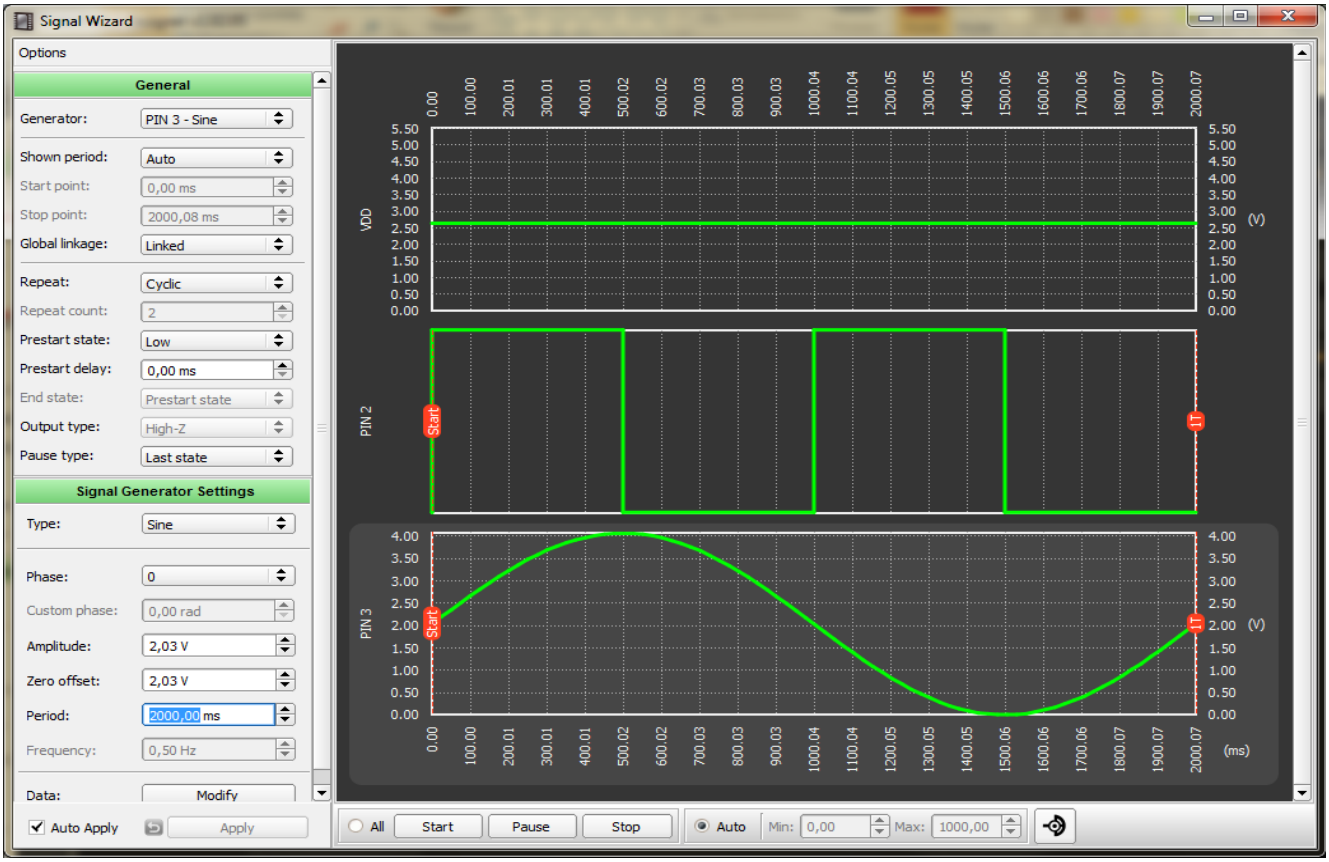


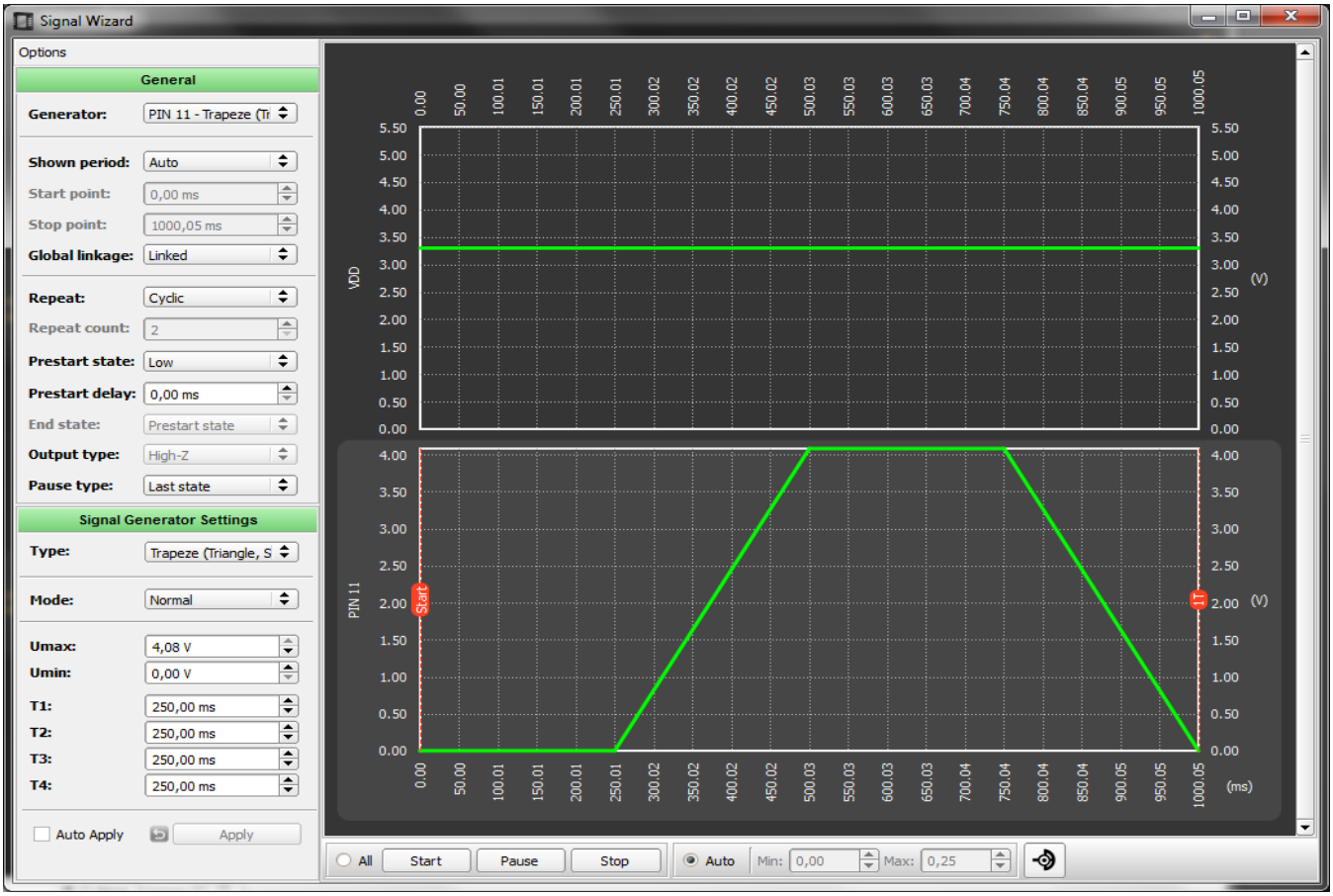
Figure 10-25. Sine



Sine settings:

Repeat:	One shot/Cyclic/Custom	- repeat option
Phase:	Custom/0/Pi:2/Pi/3Pi:2	- φ0
Custom phase:		- show phase in a radian
Amplitude:		- amplitude
Zero offset:		- zero offset
Period:		- period
Frequency:		- shows frequency
Data:		- change signal using Custom Signal Wizard

Figure 10-26. Trapezoid (Triangle, Sawtooth)



Trapeze Settings:

Mode:	Normal/Invert	-signal mode
Umax/Umin		-max/min voltage level
T1, T2, T3, T4		-duration of trapezoid

If T_3 = 1 signal is a triangle.
If T_3 = 1, T_2 = 2 or T_4 = 2 signal is a saw.

Figure 10-27. Duration of Trapezoid

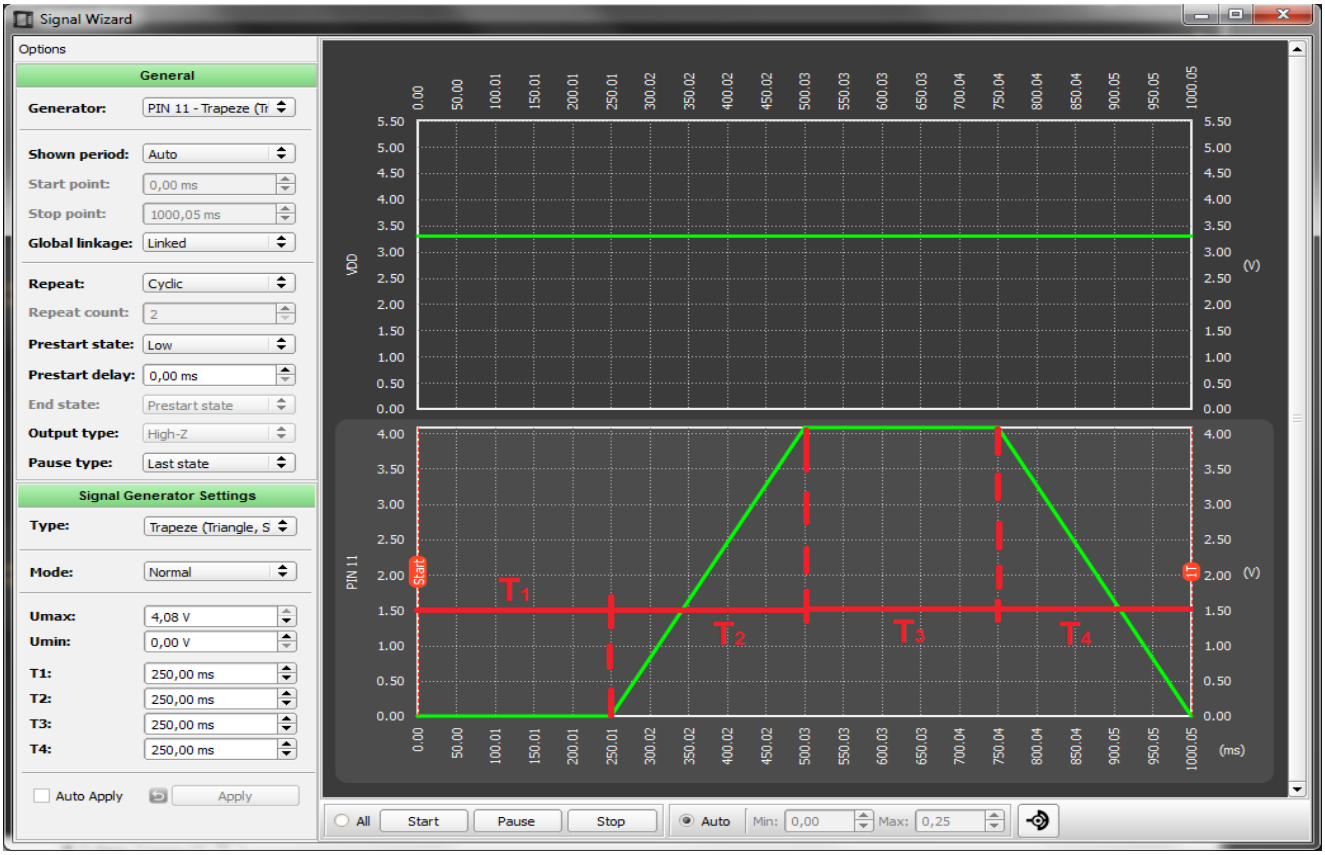
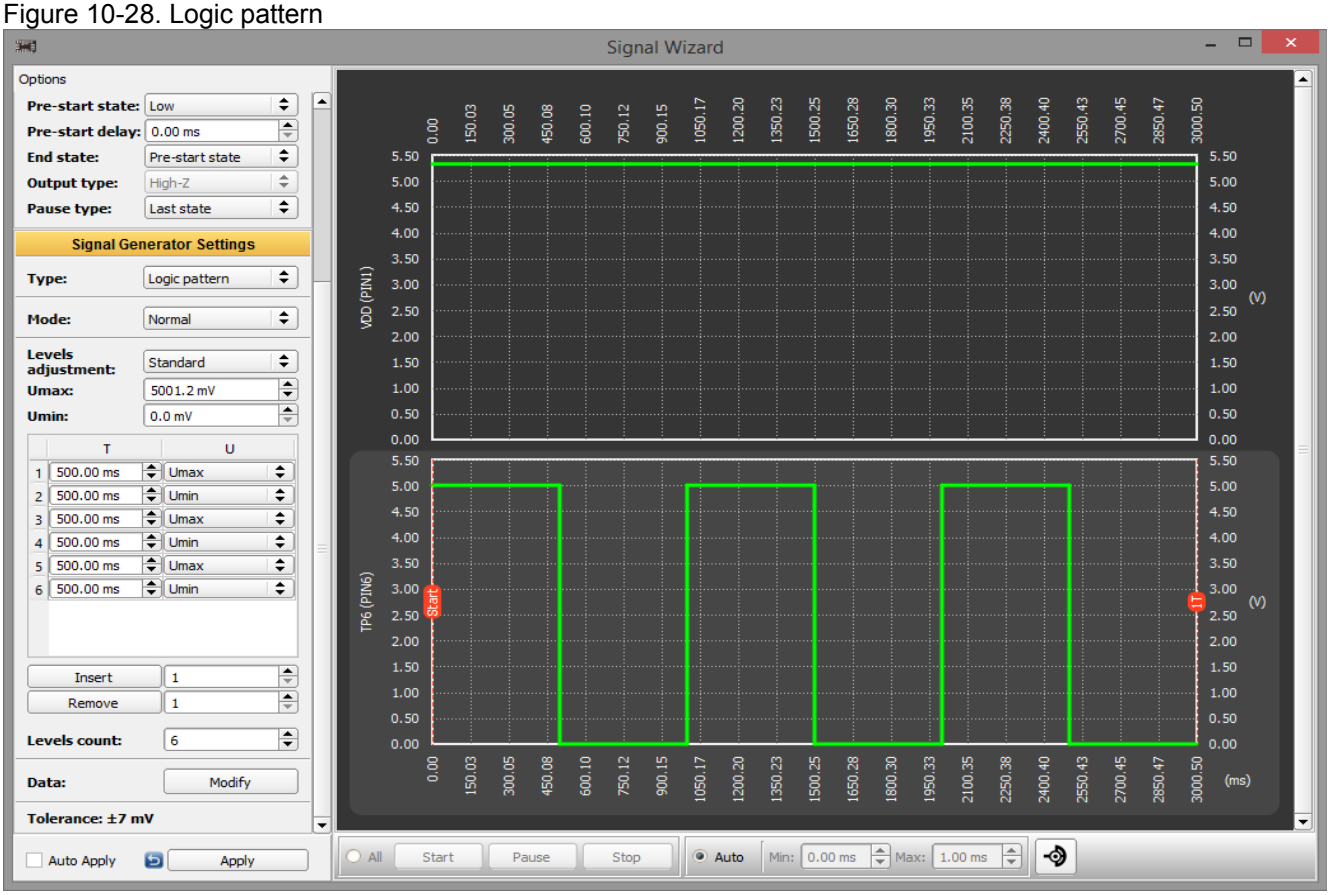


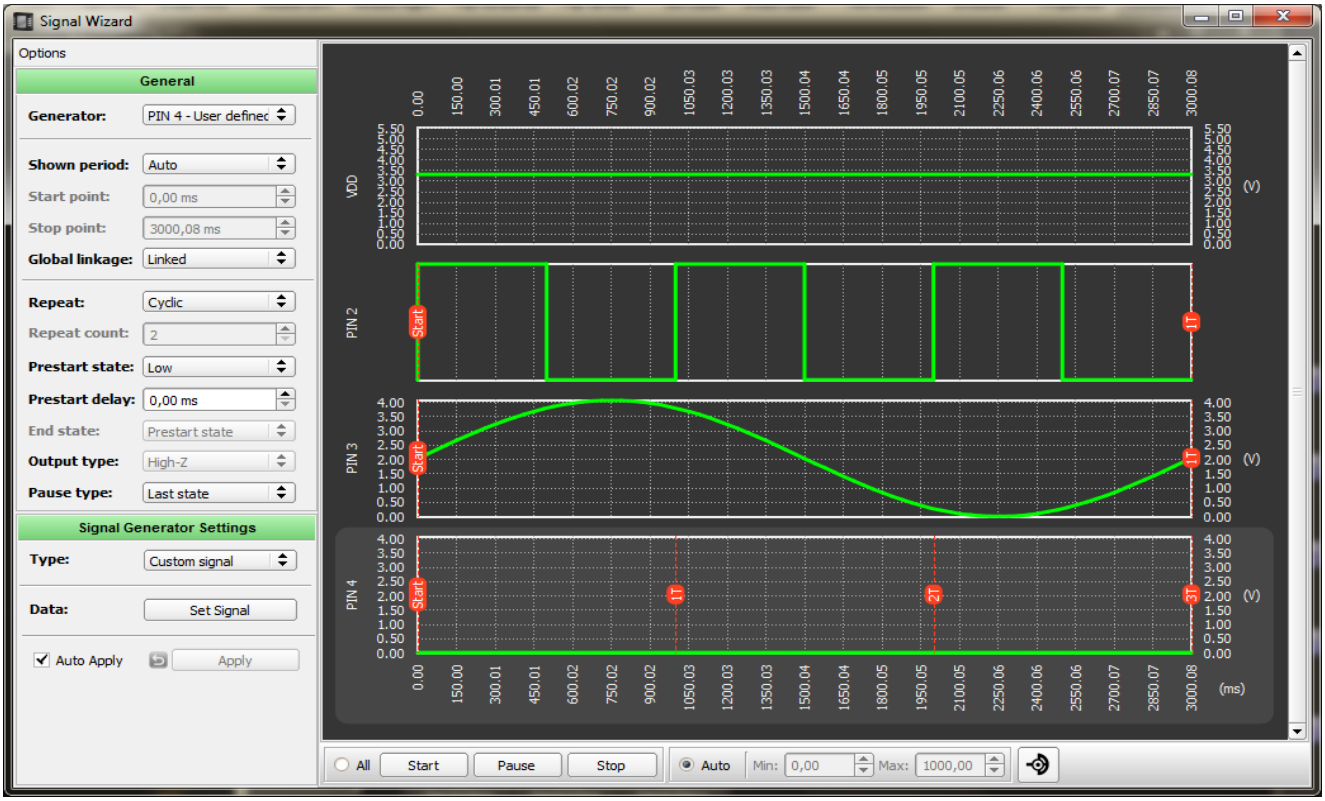
Figure 10-28. Logic pattern



Configuration options:

Mode:	Normal/Invert	- signal mode
Repeat:	One shot/Cyclic/Custom	- repeat option
T/Level:		- sets duration of level
Insert:		- insert pulse to the entered position;
Remove:		- remove pulse from the entered position;
Count:		- pulse count

Figure 10-29. Custom Signal (Arbitrary waveform)

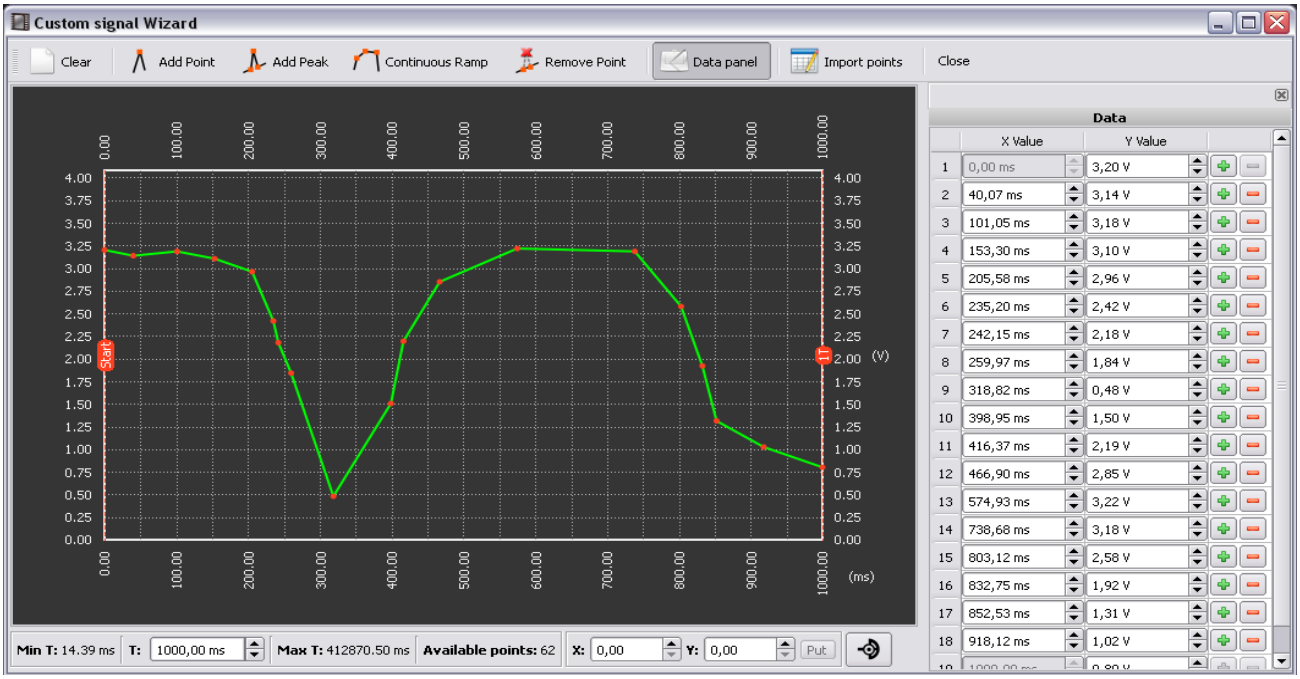


Custom Signal Settings:

Repeat:	One shot/Cyclic/Custom	- repeat option;
Data:	Set Signal	- change signal using Custom Signal Wizard

10.2.5. Custom Signal Wizard

Figure 10-30. Drawing Signal (Arbitrary waveform)



Toolbar:

Clear	- clear data
Add Point/Add Peak/Continuous Ramp/Remove Point	- draw mode
Data panel	- turn on/off the data table
Import points	- copy points from another application
Close	- close window with current signal

Figure 10-31. Peak

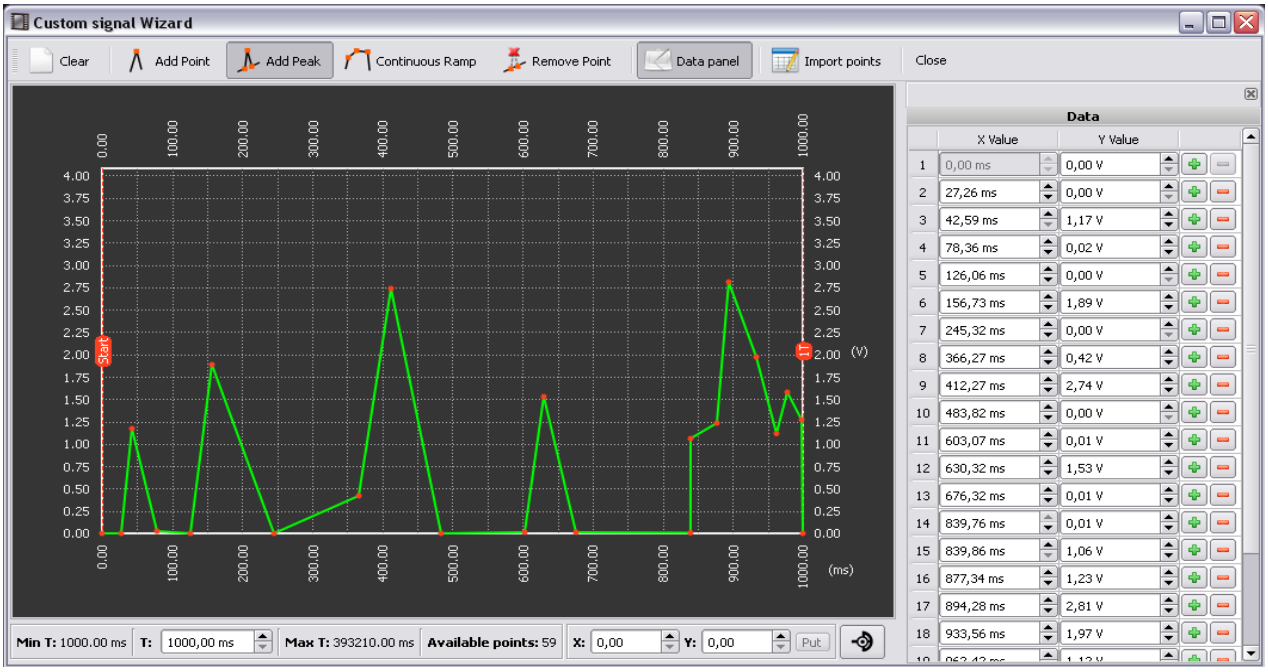
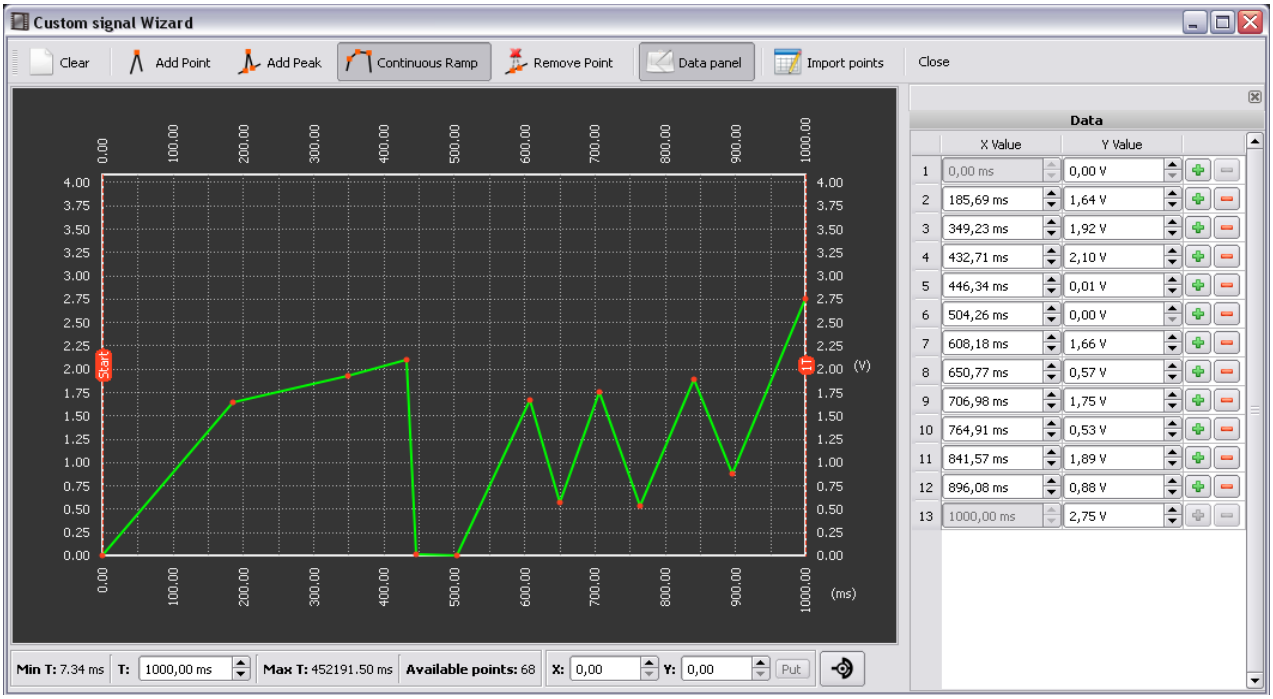
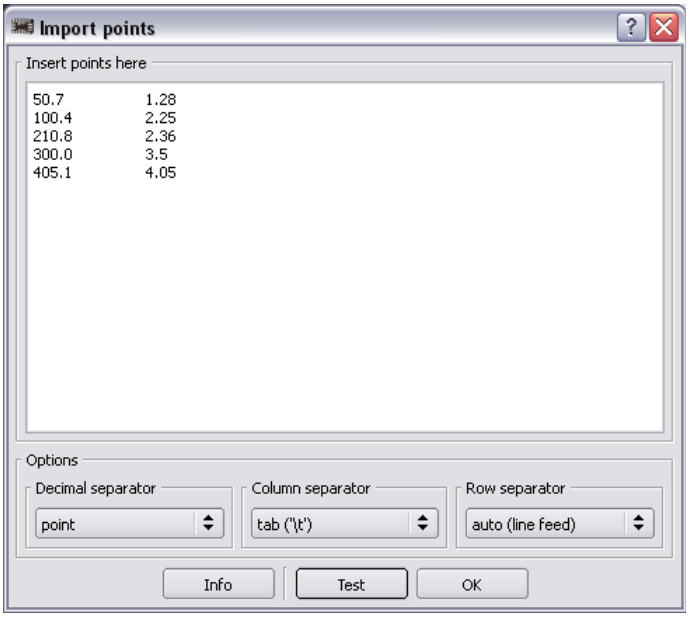


Figure 10-32. Continuous Ramp



Remove Point: Removes selected point. Double-clicking on the point will also remove it.
Data panel: Turns on/off the data table. User can remove/change values for selected point or add new point between two existing points.

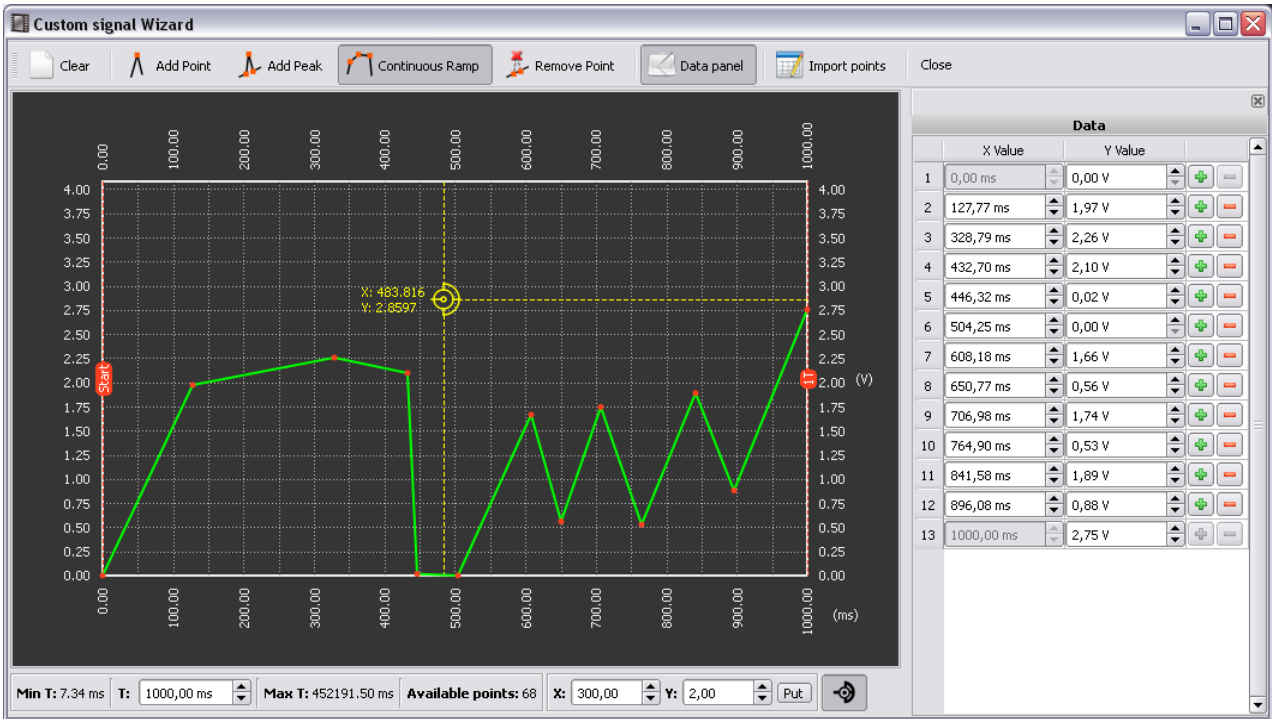
Figure 10-33. Import Points



User can insert points from another application and set separators options:
Decimal separator: point/comma;
Column separator: auto/tab(“\t”)/other;
Row separator: auto(line feed)/ tab(“\t”)/other;

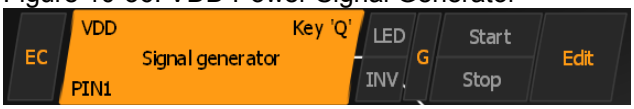
Figure 10-34. Data Panel

Figure 10-35. Cursor



10.2.6. VDD Power Signal Generator

Figure 10-36. VDD Power Signal Generator



Simple signal generator for VDD with its own options.

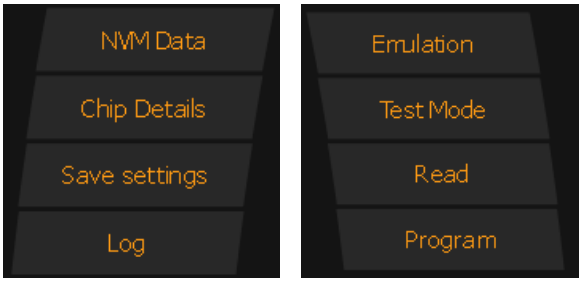
10.3. Expansion Connector

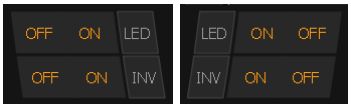
User can connect/disconnect I/O pads of GreenPAK with the expansion connector on the board.

Figure 10-37. Expansion Connector

10.4. Control panel

Figure 10-38. Control Panel



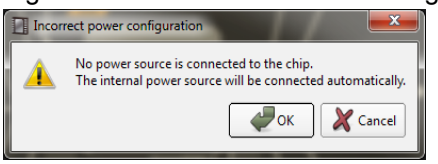


Emulation:

The current project will be loaded to the chip (but not programmed), and will be ready for test on the emulation board. Also, user can change any configuration during the emulation process.

In the case when Power key and VDD key on the Expansion connector are turned off, a warning message will pop up (figure 10-39).

Figure 10-39. Incorrect Power Configuration


Incorrect power configuration
No power source is connected to the chip.
The internal power source will be connected automatically.
OK
Cancel

Test mode:

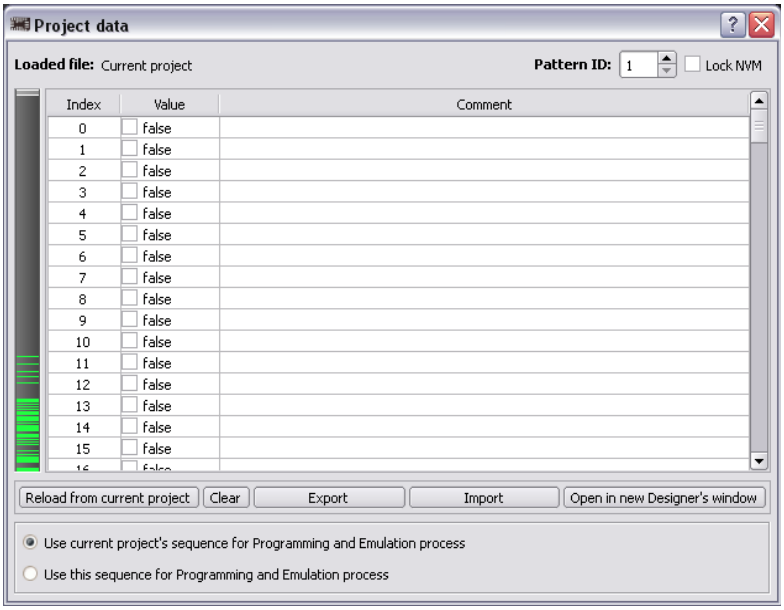
Test mode is used for connecting or disconnecting the chip's I/O pads to stimulus areas, configured by user. Also, a user can check the programmed chip using the test mode without emulation. In order to do this one only needs to turn on the test mode and power key. The test mode can work without power on the chip. User will control the Power key manually.

Read:

Read chip using emulation board.

Program:
Program chip with the current project.
NVM Data:
The table of bits.
Pattern ID – gives an ID (1-255) to the project. The ID will be put in the chip after programming, and also will be read back while in “chip reading” operation.
Lock NVM – blocks NVM reading. A programmed project becomes unavailable for chip reading. The chip is still available for emulation.
Use current project’s sequence for Programming end Emulation process – user can choose to use current project's sequence for programing and emulation process.
Use this sequence for Programming end Emulation process – user can choose current sequence for programming and emulation process.
Reload from current project – user can load bit sequence from current project.
Clear – sets all bits to false.
Export – save data to text file.
Import – load data from text file.
Open in new Designer's window – open current bit sequence in new Designer’s window.

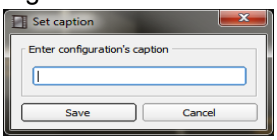
Figure 10-40. NVM Data



Chip Details:
Show details about chip and board.

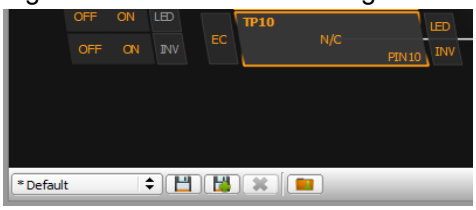
Save settings:
Save current configuration of a test mode to the project file.

Figure 10-41. Save Settings dialog



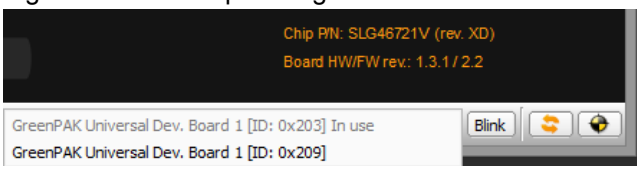
Log:
Show log.
LED control:
User can turn on/off leds on GreenPAK emulation board.
Test mode configuration:
- Save current configuration of a test mode to the project file
- Delete selected configuration
- Import new configuration(s) from project file(s).

Figure 10-42. Test Mode Configuration



Support for multiple devices:
This feature allows user to connect few supported hardware boards and select specific one for performing the operations.

Figure 10-43. Multiple Silego devices

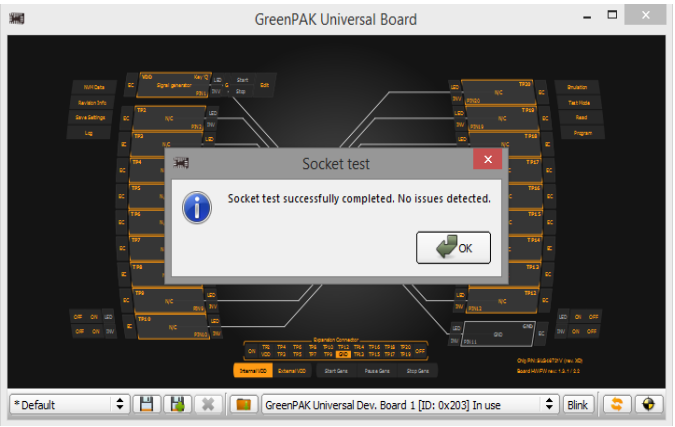

Chip P/N: SLG46721V (rev. XD)
Board HW/FW rev.: 1.3.1 / 2.2
GreenPAK Universal Dev. Board 1 [ID: 0x203] In use
GreenPAK Universal Dev. Board 1 [ID: 0x209]
Blink

Blink:
Selected board blinks to notify its selection
Refresh button:
Refresh button updates chip information in bottom right corner of the Emulator.

Socket Test:

This feature allows testing the socket connectors to ensure that it works properly and doesn't have influence on emulation or reading/programming processes.

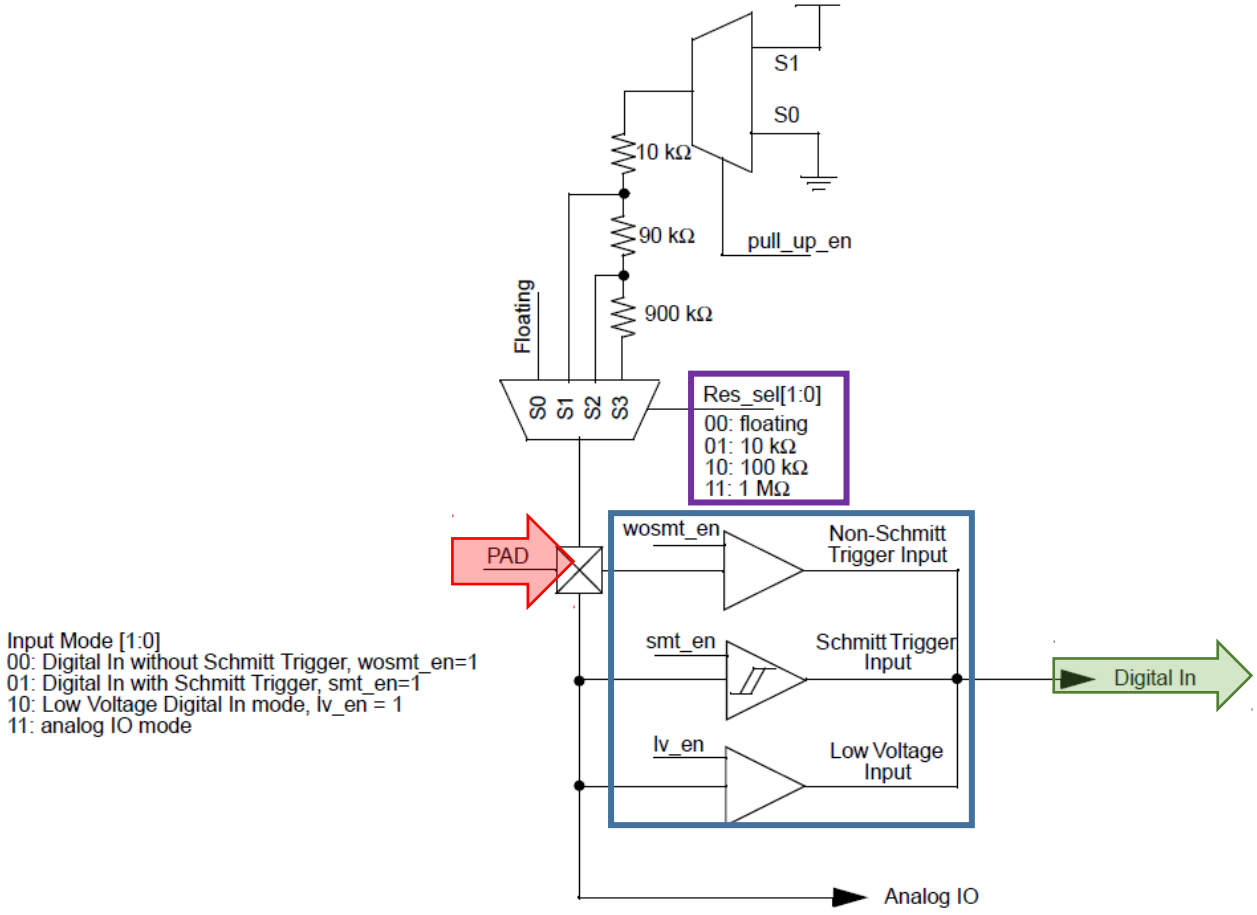
Figure 10-44. Socket Test Results



11. Designing Overview

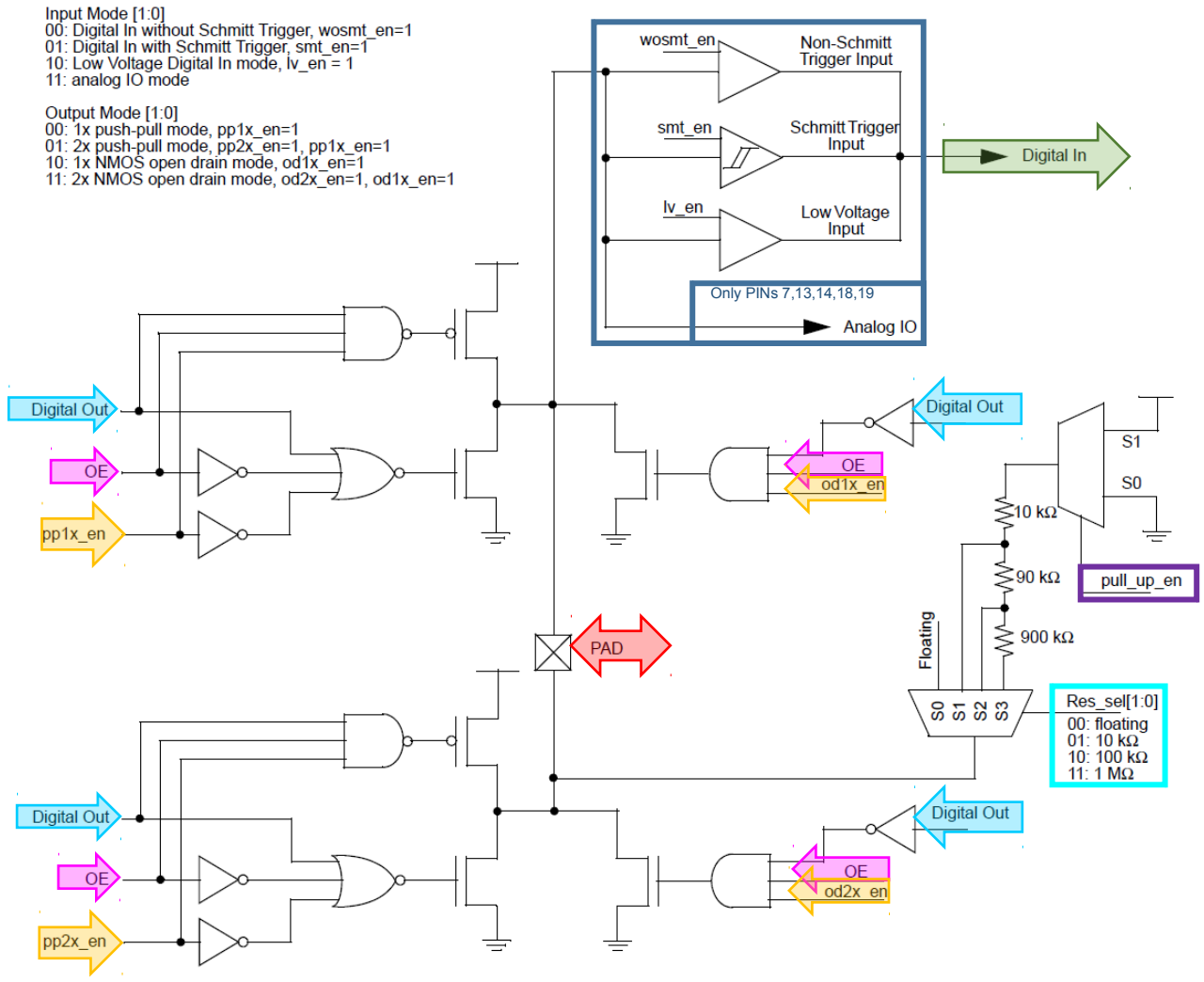
11.1. SLG4672x Properties Interpretation

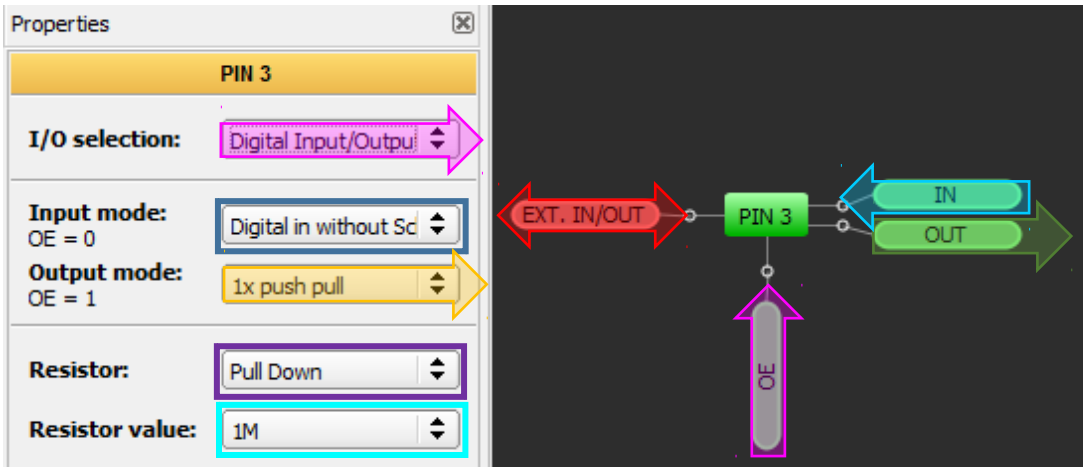
Pin2



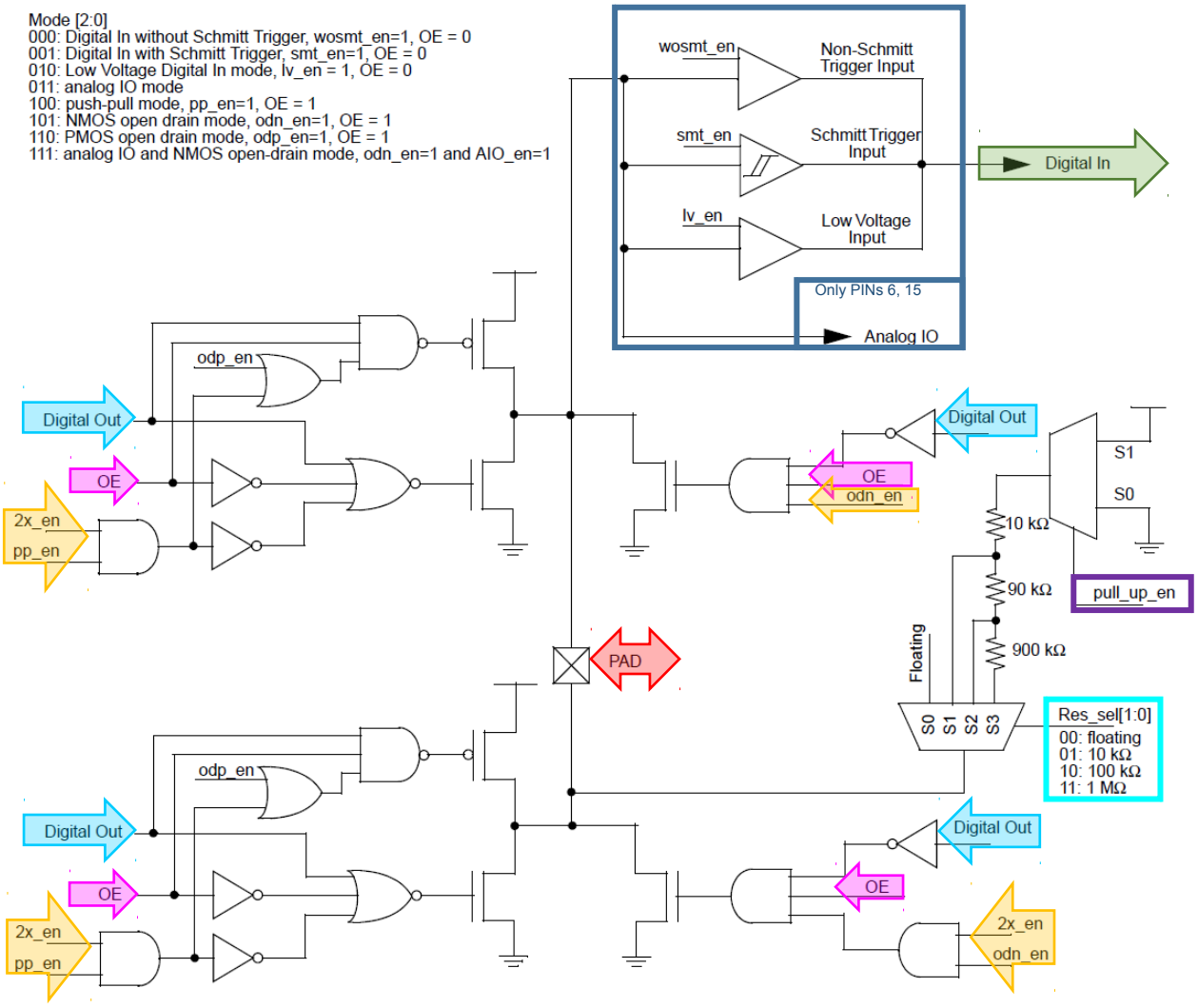
Properties
PIN 2
I/O selection:
Digital Input
Input mode:
OE = 0
Digital in without Sc
Output mode:
OE = 1
None
Resistor:
Pull Down
Resistor value:
1M
EXT. IN
PIN 2
OUT

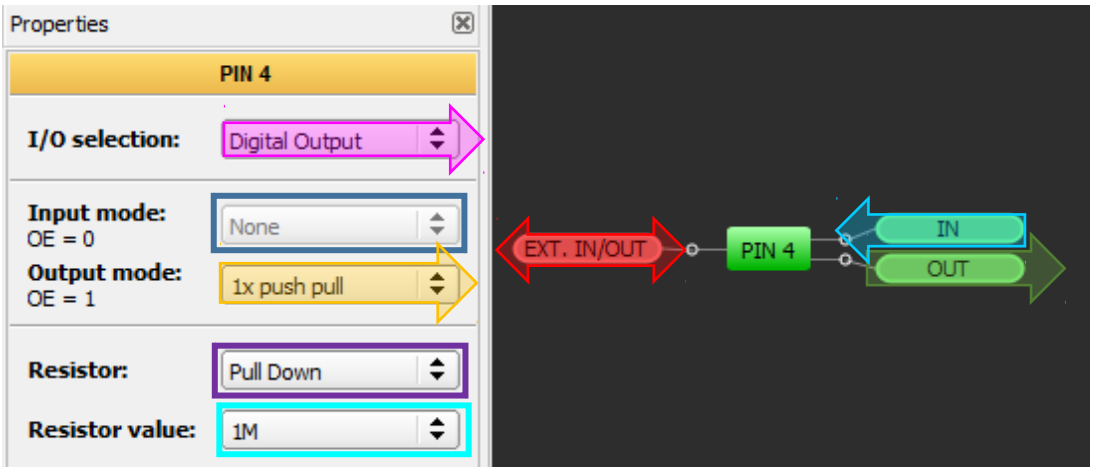
Matrix OE IO Structure (for Pins 3, 5, 7, 9, 13, 14, 16, 18, 19)



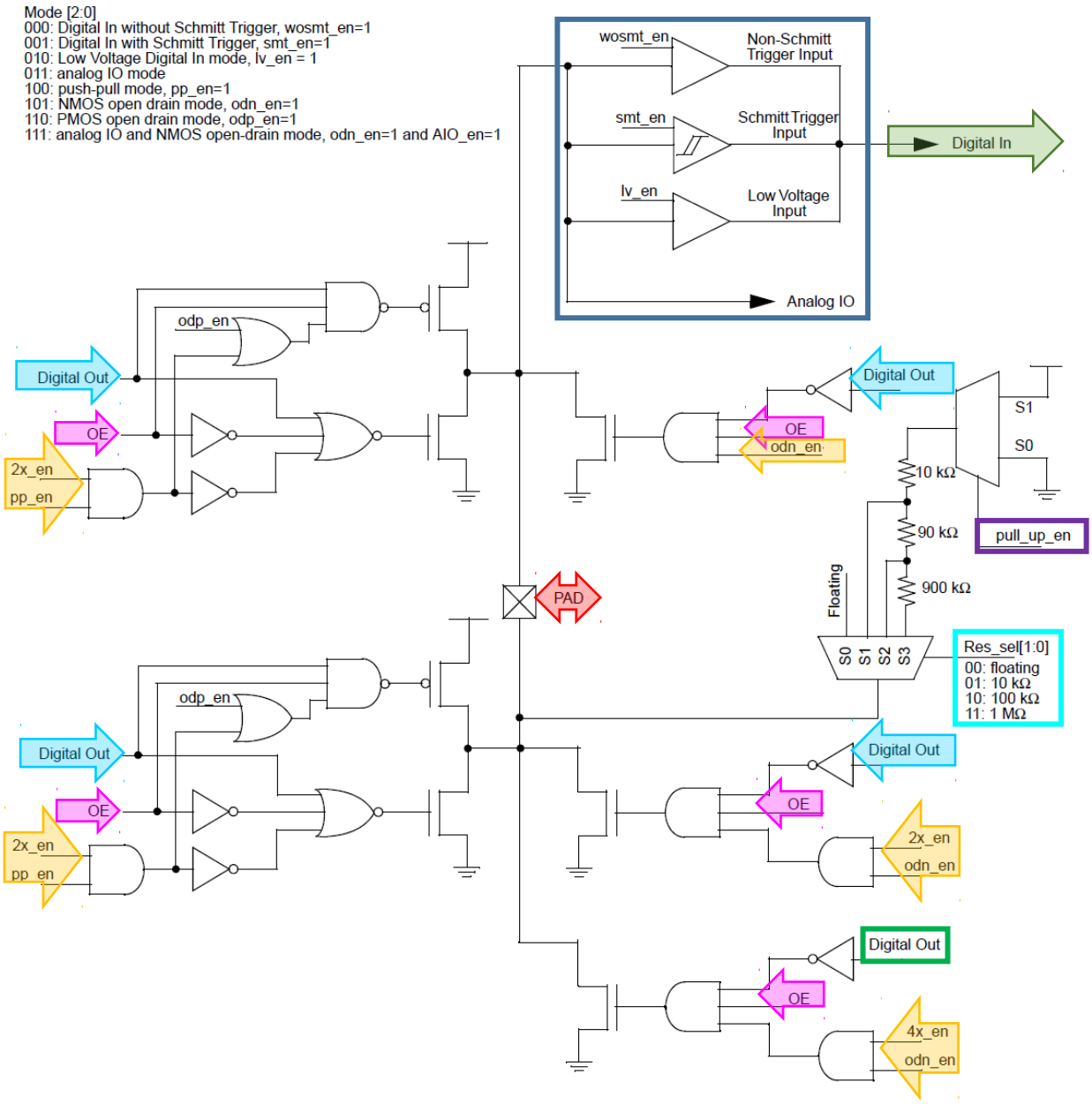

Properties
PIN 3
I/O selection:
Digital Input/Outpu
Input mode:
OE = 0
Digital in without Sc
Output mode:
OE = 1
1x push pull
Resistor:
Pull Down
Resistor value:
1M
EXT. IN/OUT
PIN 3
IN
OUT
OE

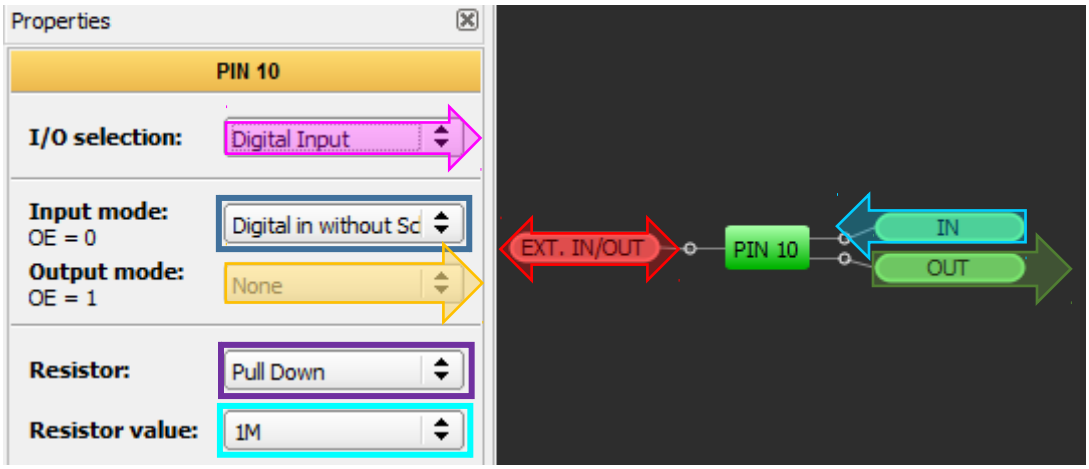
Register OE IO Structure (for Pins 4, 6, 8, 15, 17, 20)



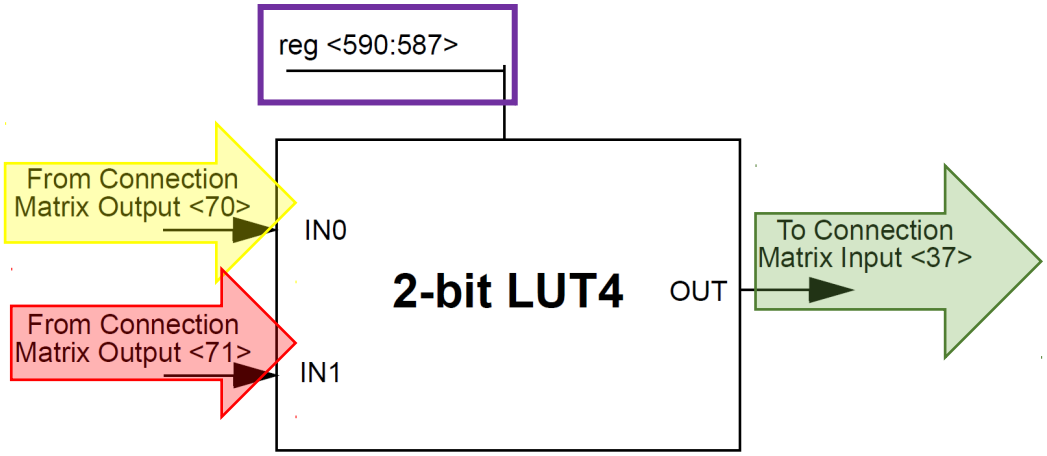

Properties
PIN 4
I/O selection:
Digital Output
Input mode:
OE = 0
None
Output mode:
OE = 1
1x push pull
Resistor:
Pull Down
Resistor value:
1M
EXT. IN/OUT
PIN 4
IN
OUT

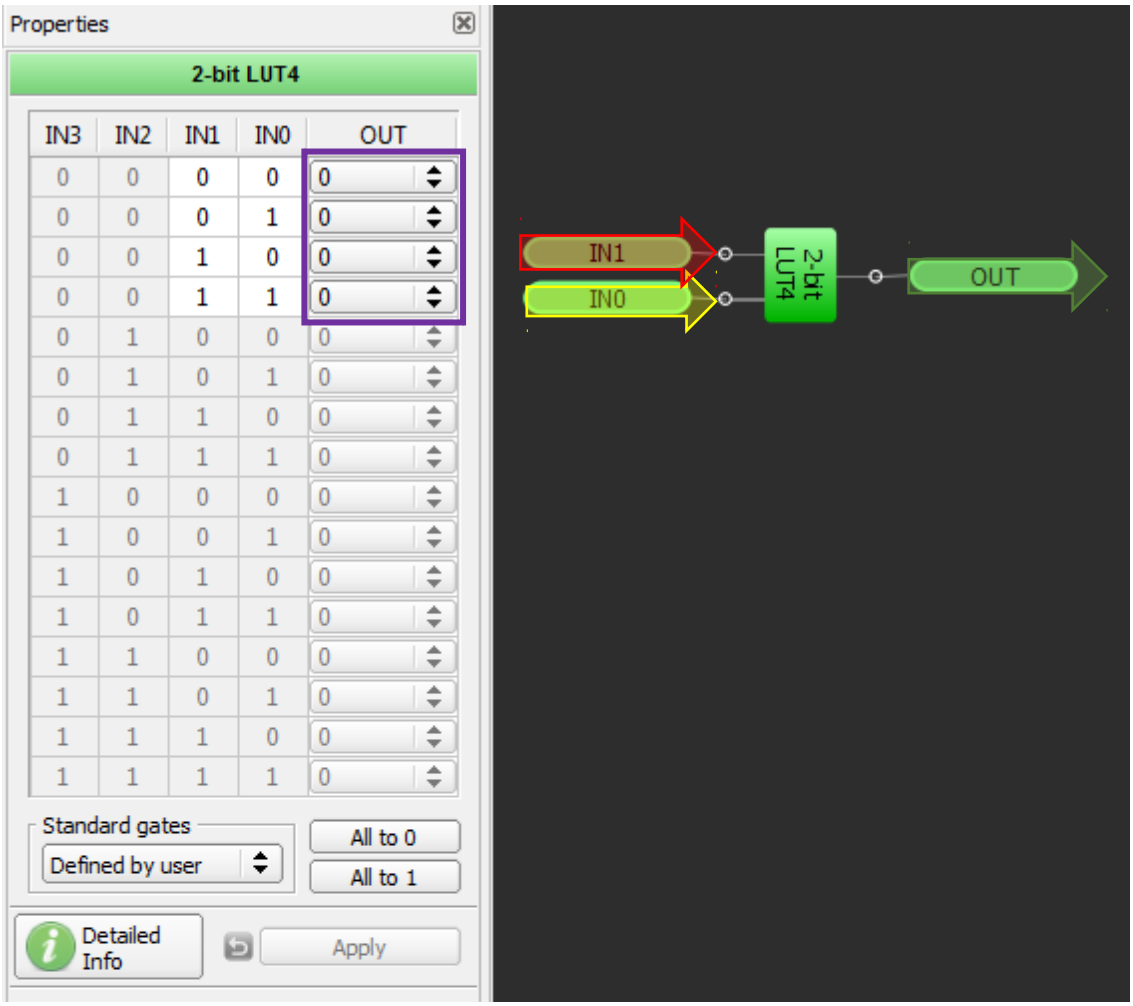
Register OE IO Structure with Super Driver (for Pins 10, 12)



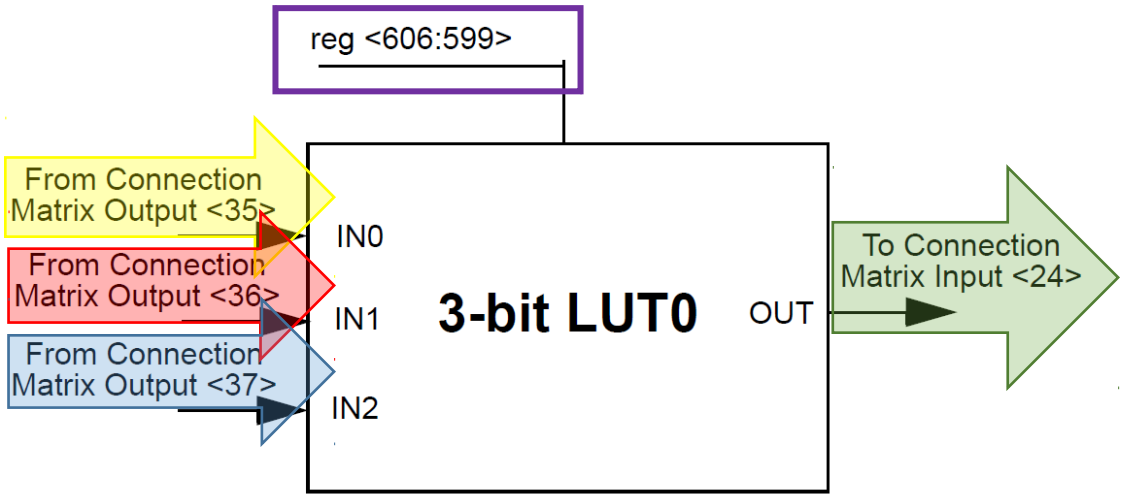

Properties
PIN 10
I/O selection:
Digital Input
Input mode:
OE = 0
Digital in without Sc
Output mode:
OE = 1
None
Resistor:
Pull Down
Resistor value:
1M
EXT. IN/OUT
PIN 10
IN
OUT

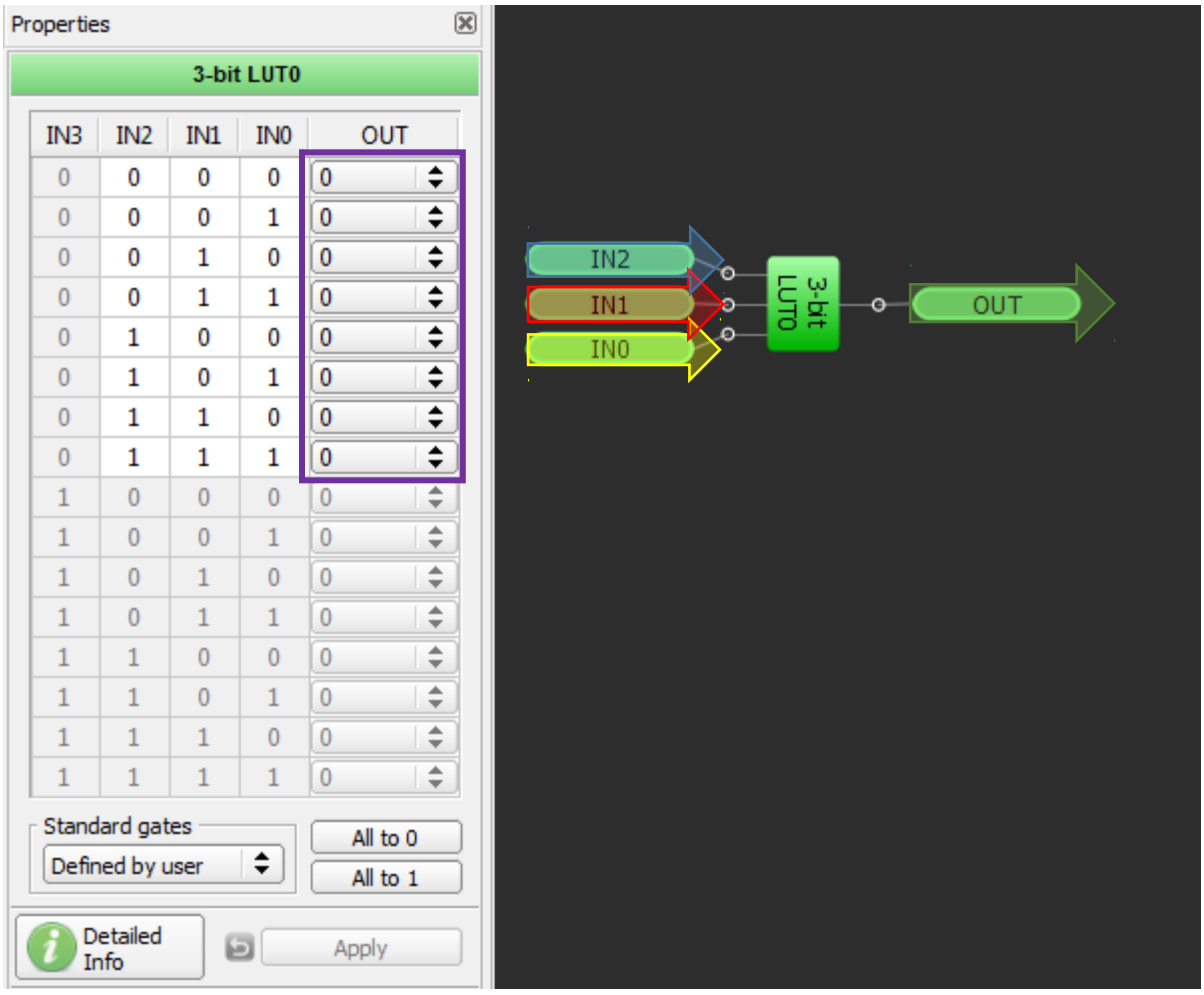
2-Bit LUT


reg <590:587>
From Connection Matrix Output <70>
From Connection Matrix Output <71>
IN0
IN1
2-bit LUT4
OUT
To Connection Matrix Input <37>

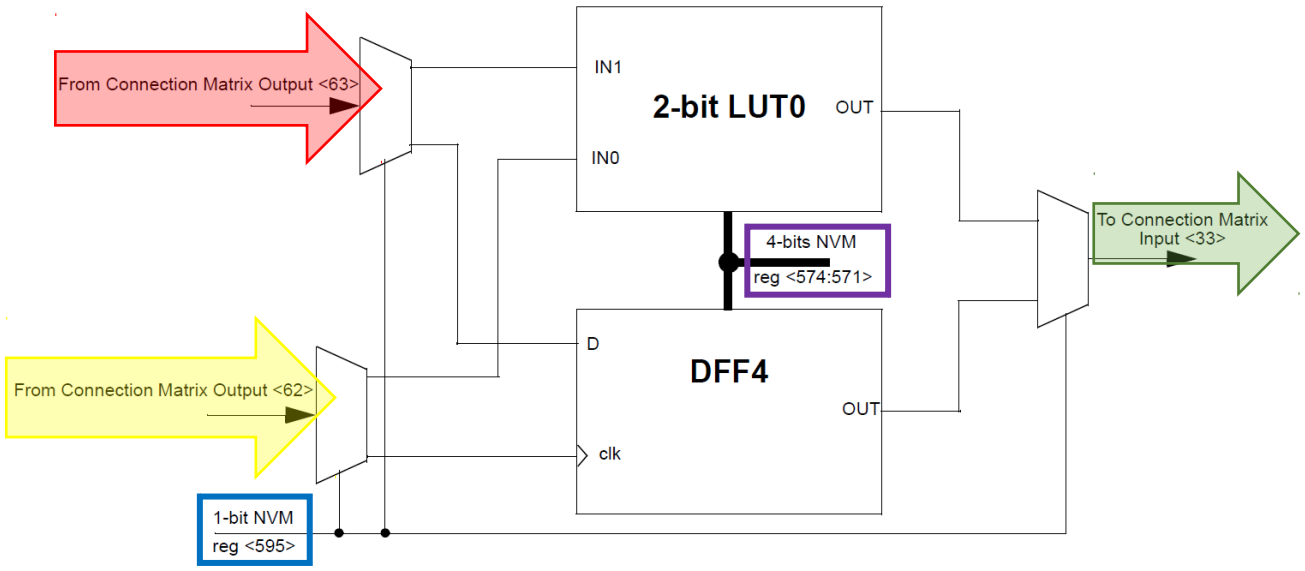

Properties
2-bit LUT4
IN3 IN2 IN1 IN0 OUT
0 0 0 0 0
0 0 0 1 0
0 0 1 0 0
0 0 1 1 0
0 1 0 0 0
0 1 0 1 0
0 1 1 0 0
0 1 1 1 0
1 0 0 0 0
1 0 0 1 0
1 0 1 0 0
1 0 1 1 0
1 1 0 0 0
1 1 0 1 0
1 1 1 0 0
1 1 1 1 0
Standard gates
Defined by user
All to 0
All to 1
Detailed Info
Apply
IN1
IN0
2-bit LUT4
OUT

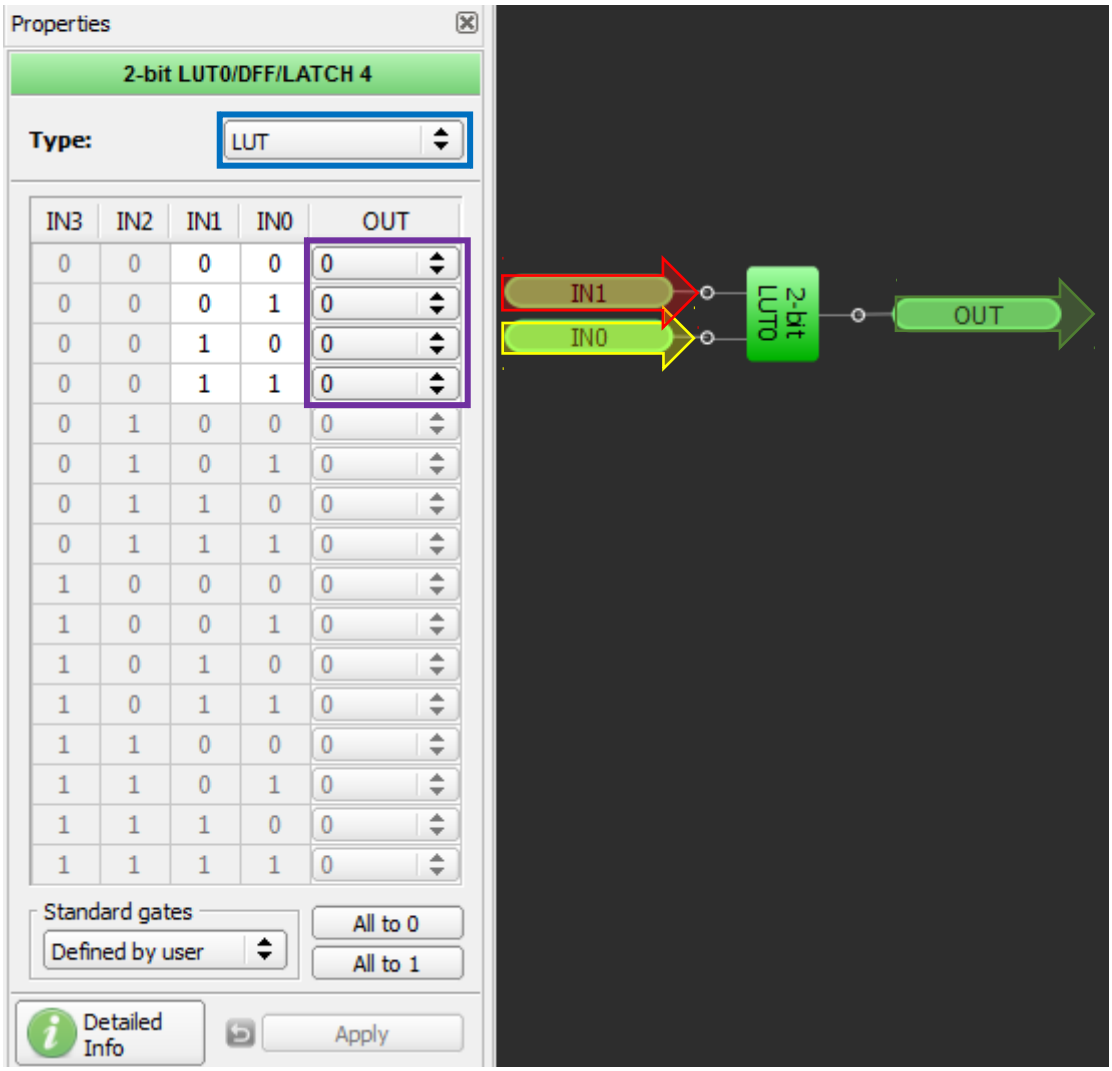
3-Bit LUT

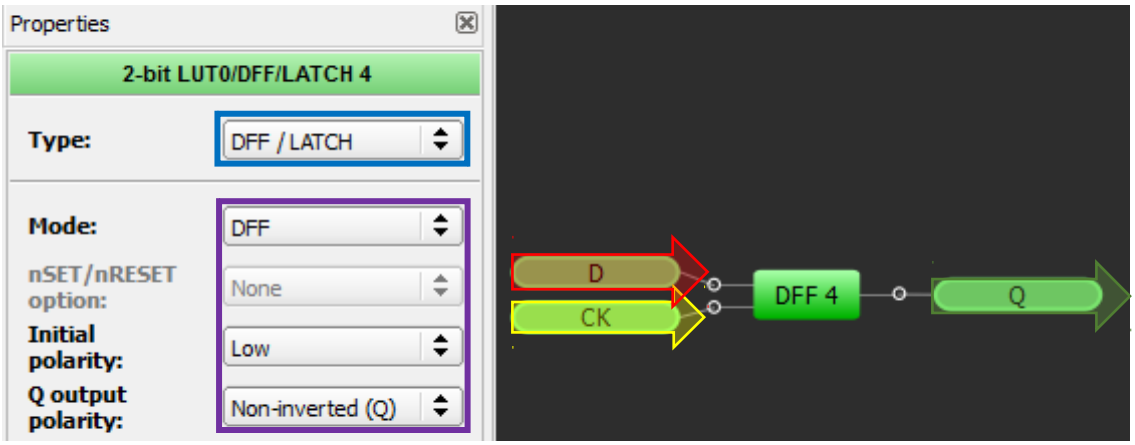

reg <606:599>
From Connection Matrix Output <35>
From Connection Matrix Output <36>
From Connection Matrix Output <37>
IN0
IN1
IN2
3-bit LUT0
OUT
To Connection Matrix Input <24>


Properties
3-bit LUT0
IN3 IN2 IN1 IN0 OUT
0 0 0 0 0
0 0 0 1 0
0 0 1 0 0
0 0 1 1 0
0 1 0 0 0
0 1 0 1 0
0 1 1 0 0
0 1 1 1 0
1 0 0 0 0
1 0 0 1 0
1 0 1 0 0
1 0 1 1 0
1 1 0 0 0
1 1 0 1 0
1 1 1 0 0
1 1 1 1 0
Standard gates
Defined by user
All to 0
All to 1
Detailed Info
Apply
IN2
IN1
IN0
3-bit LUT0
OUT

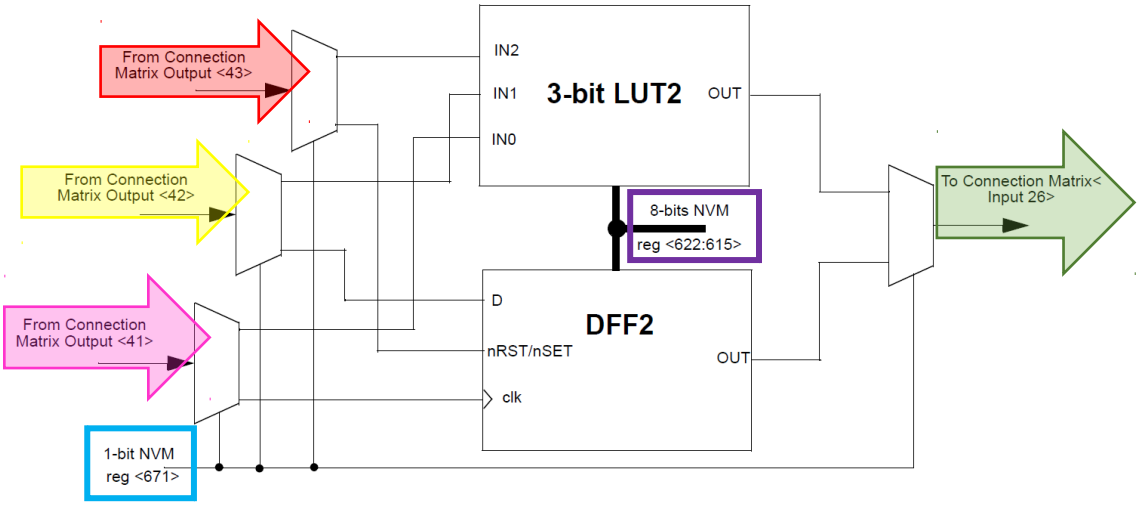
2-Bit LUT or D Flip Flop Macrocells

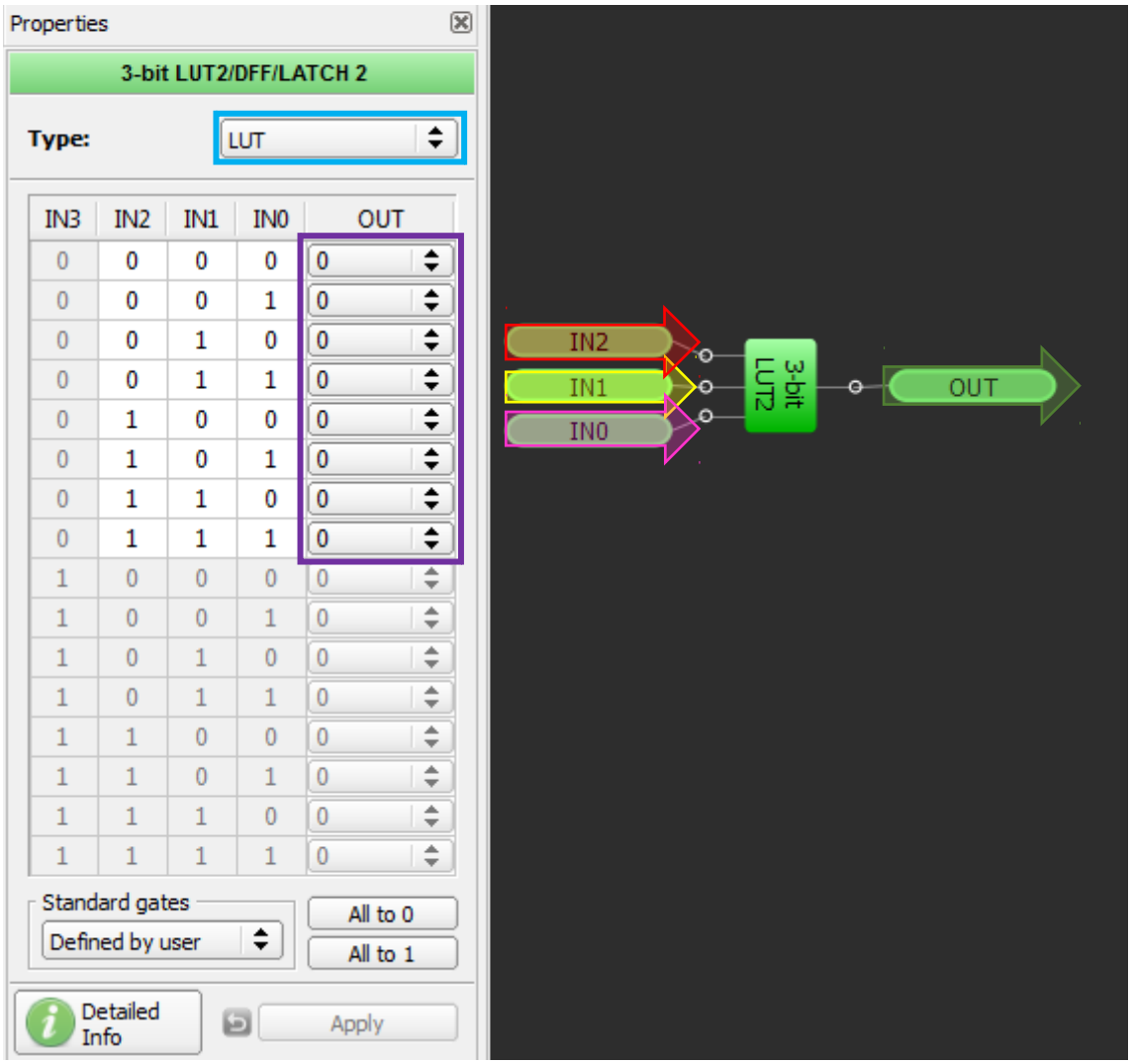


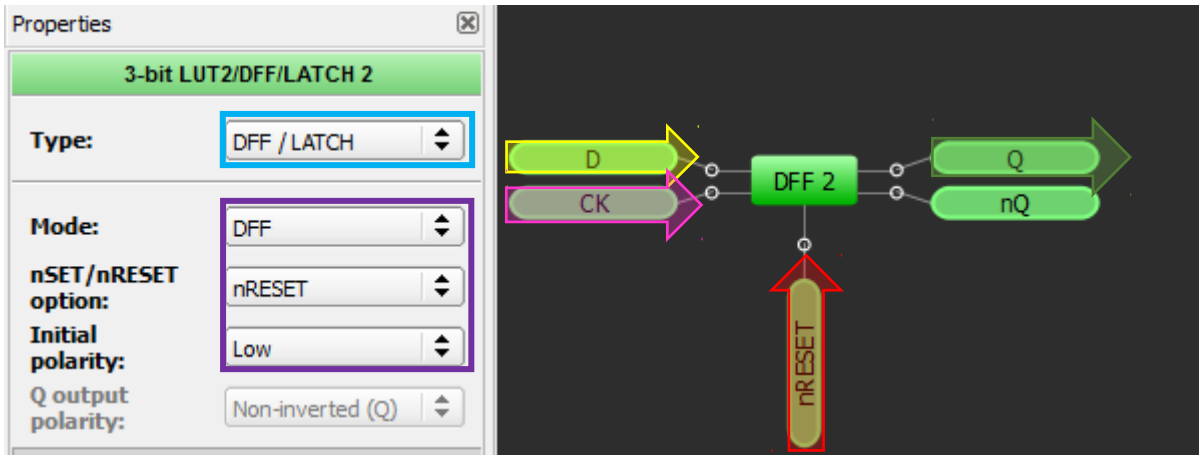

Properties
2-bit LUT0/DFF/LATCH 4
Type:
LUT
IN3 IN2 IN1 IN0 OUT
Standard gates
Defined by user
All to 0
All to 1
Detailed Info
Apply
IN1
IN0
2-bit LUT0
OUT


Properties
2-bit LUT0/DFF/LATCH 4
Type:
DFF / LATCH
Mode:
DFF
nSET/nRESET option:
None
Initial polarity:
Low
Q output polarity:
Non-inverted (Q)
D
CK
DFF 4
Q

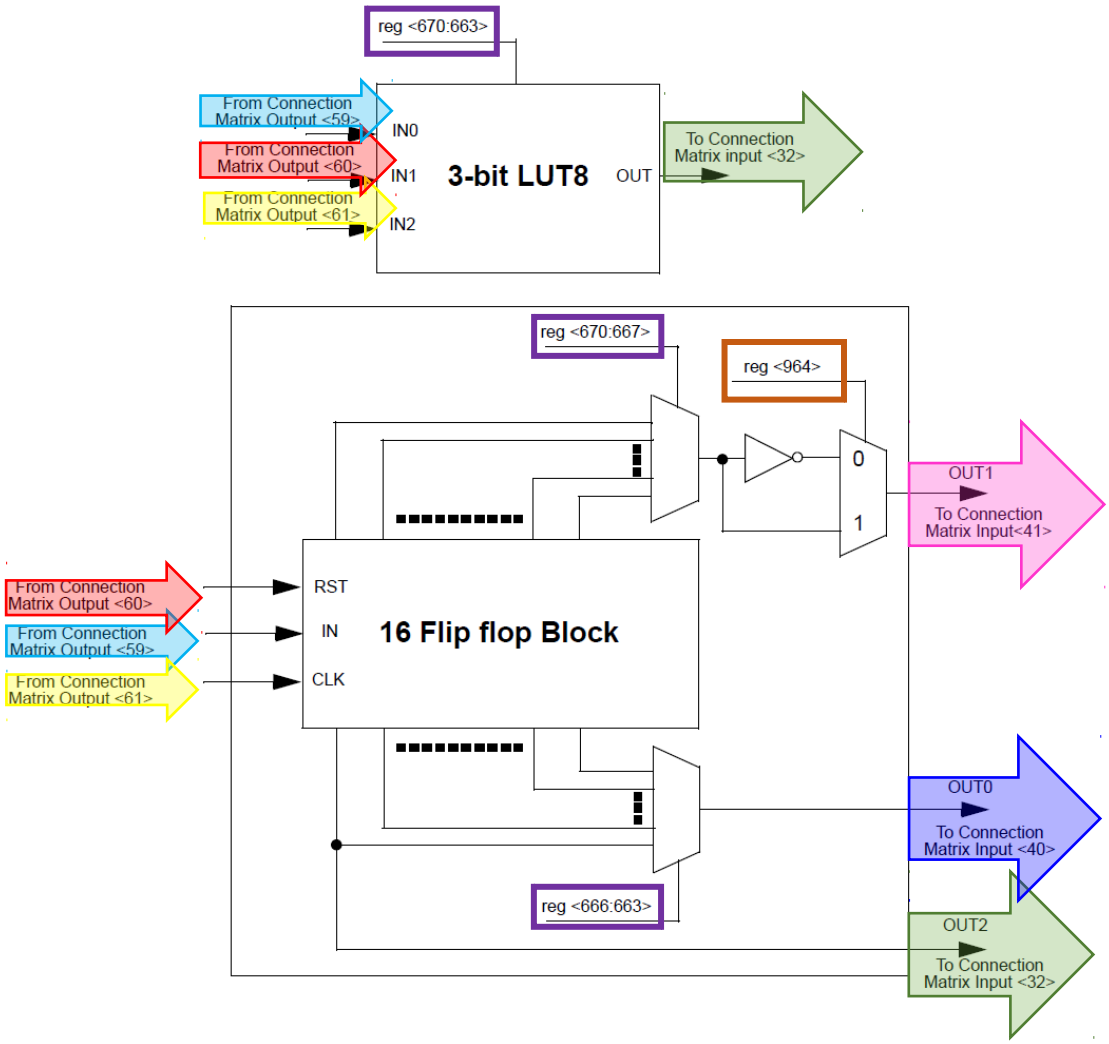
3-Bit LUT or D Flip Flop with Set/Reset Macrocells

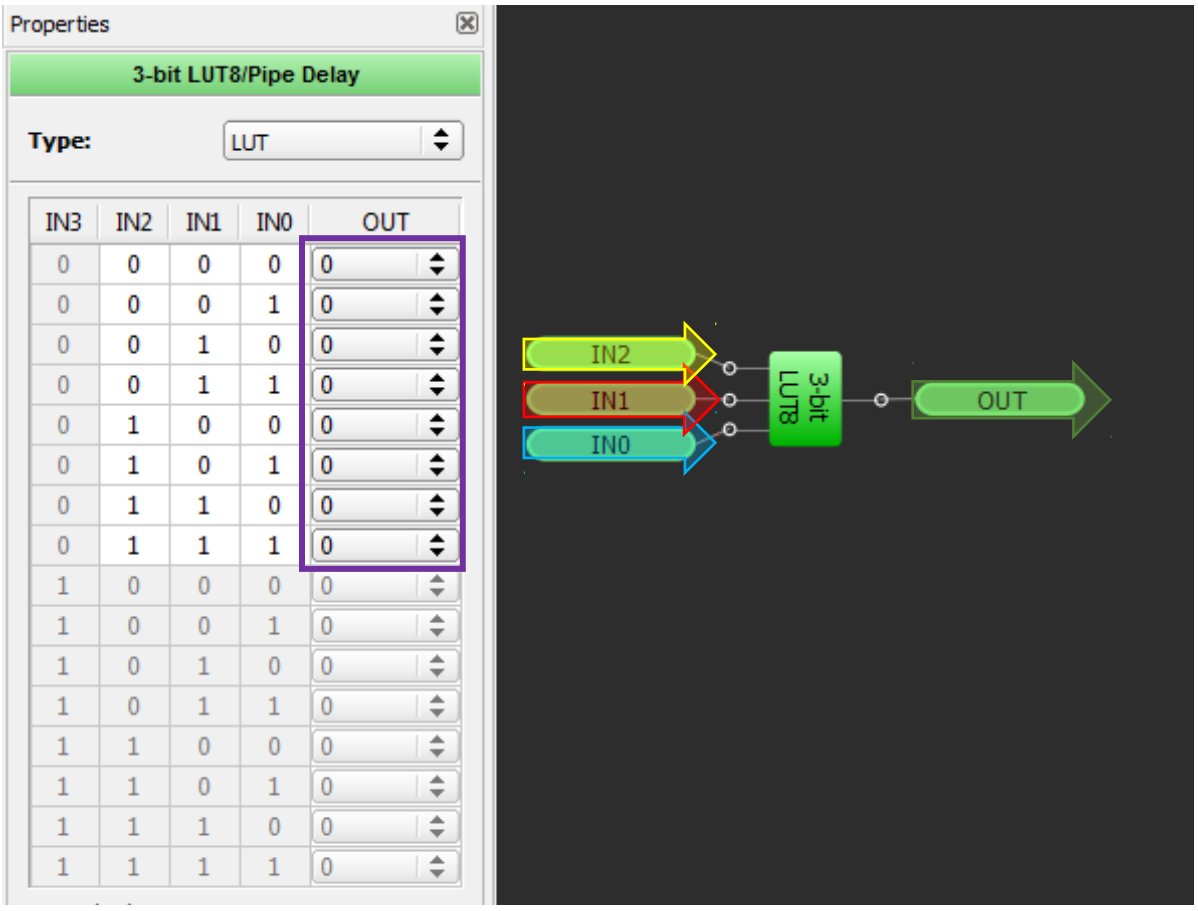


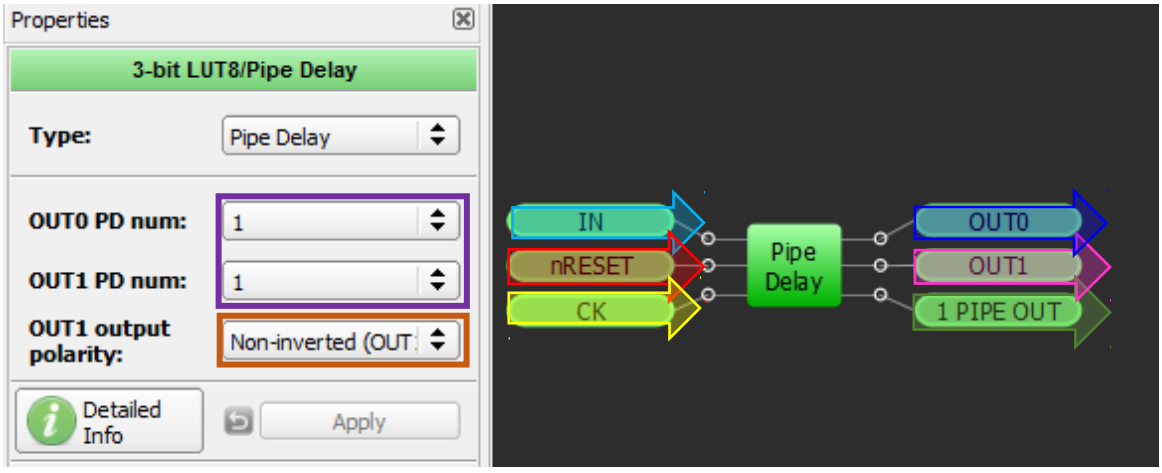

Properties
3-bit LUT2/DFF/LATCH 2
Type:
LUT
IN3 IN2 IN1 IN0 OUT
Standard gates
Defined by user
All to 0
All to 1
Detailed Info
Apply
IN2
IN1
IN0
3-bit LUT2
OUT


Properties
3-bit LUT2/DFF/LATCH 2
Type:
DFF / LATCH
Mode:
DFF
nSET/nRESET option:
nRESET
Initial polarity:
Low
Q output polarity:
Non-inverted (Q)
D
CK
DFF 2
Q
nQ
nRESET

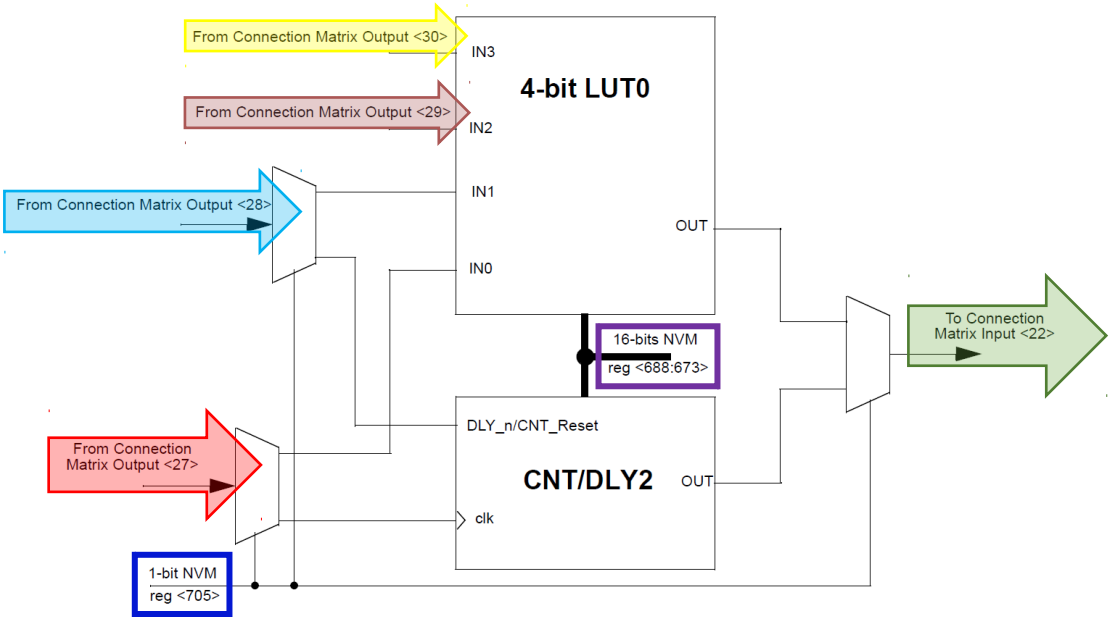
3-Bit LUT or Pipe Delay Macrocell

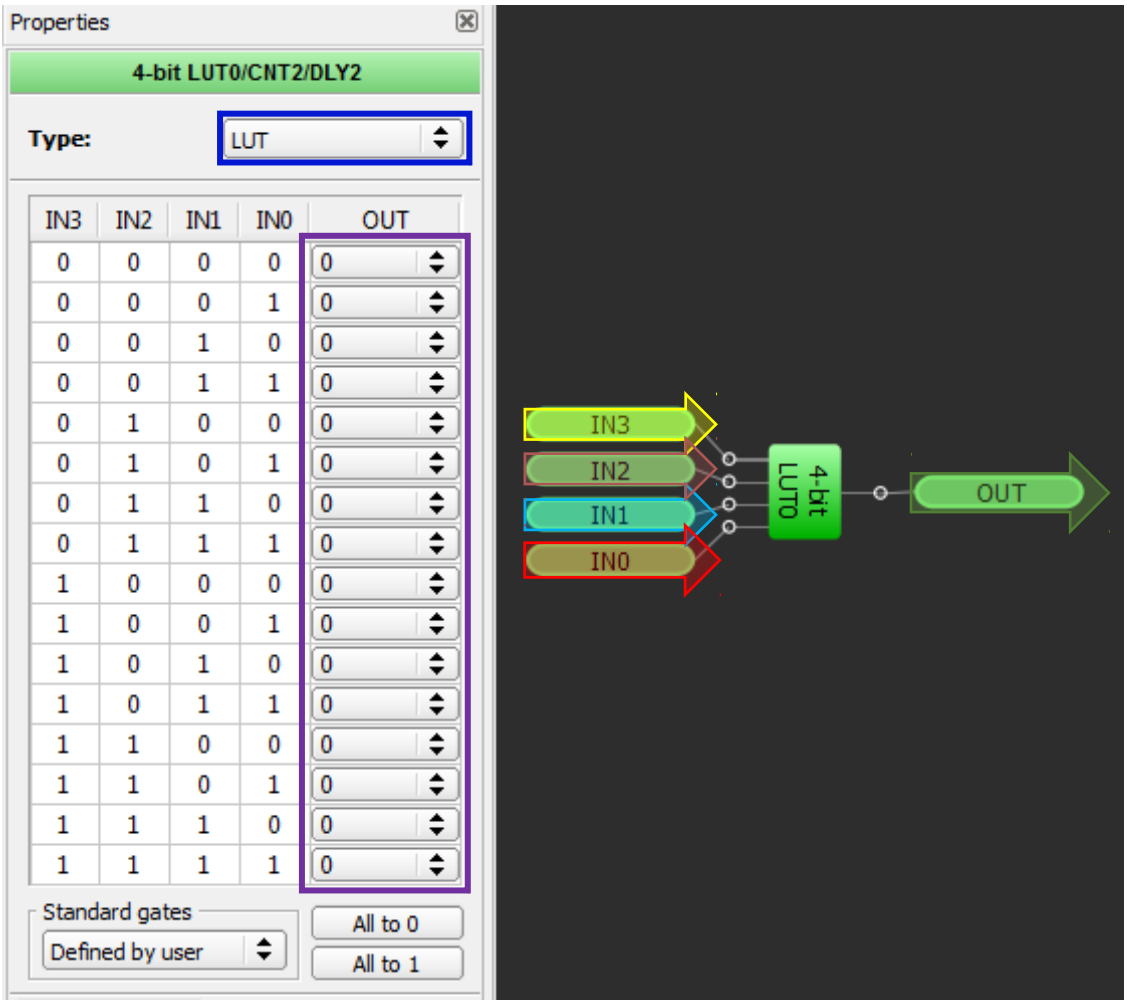


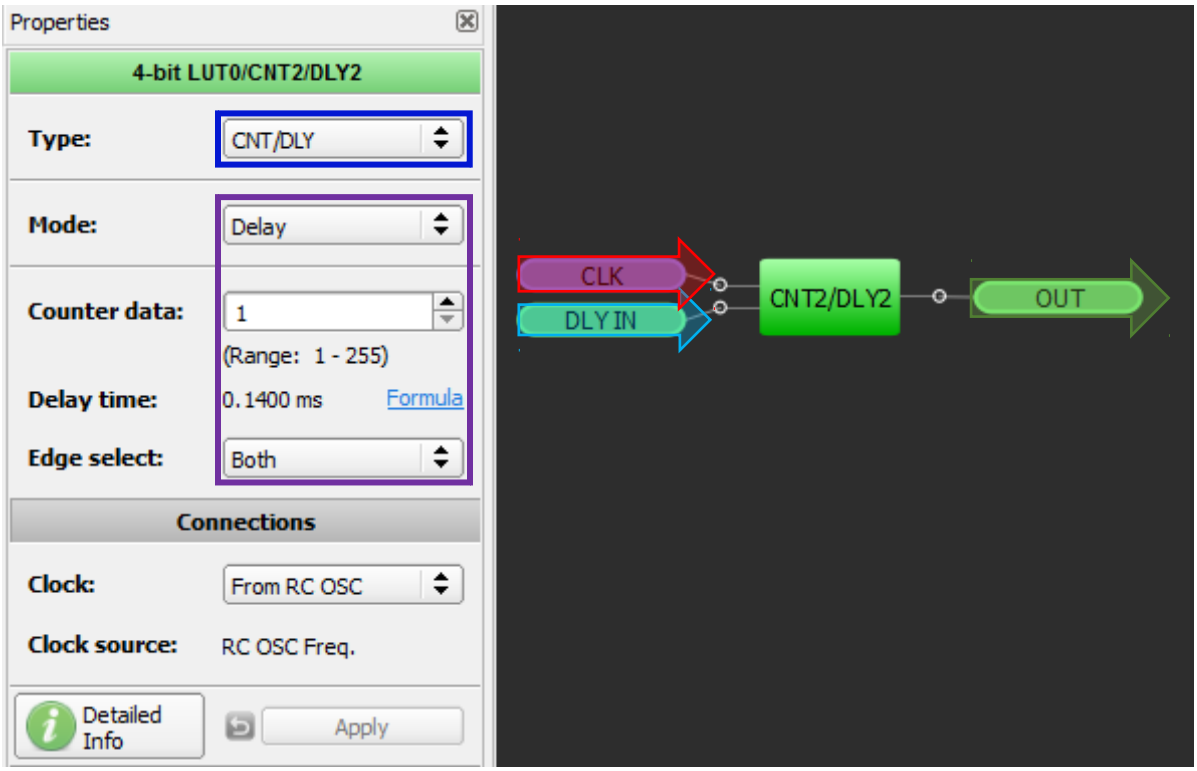

Properties
3-bit LUT8/Pipe Delay
Type:
LUT
IN3 IN2 IN1 IN0 OUT
IN2
IN1
IN0
3-bit LUT8
OUT


Properties
3-bit LUT8/Pipe Delay
Type:
Pipe Delay
OUT0 PD num:
1
OUT1 PD num:
1
OUT1 output polarity:
Non-inverted (OUT
Detailed Info
Apply
IN
nRESET
CK
Pipe Delay
OUT0
OUT1
1 PIPE OUT

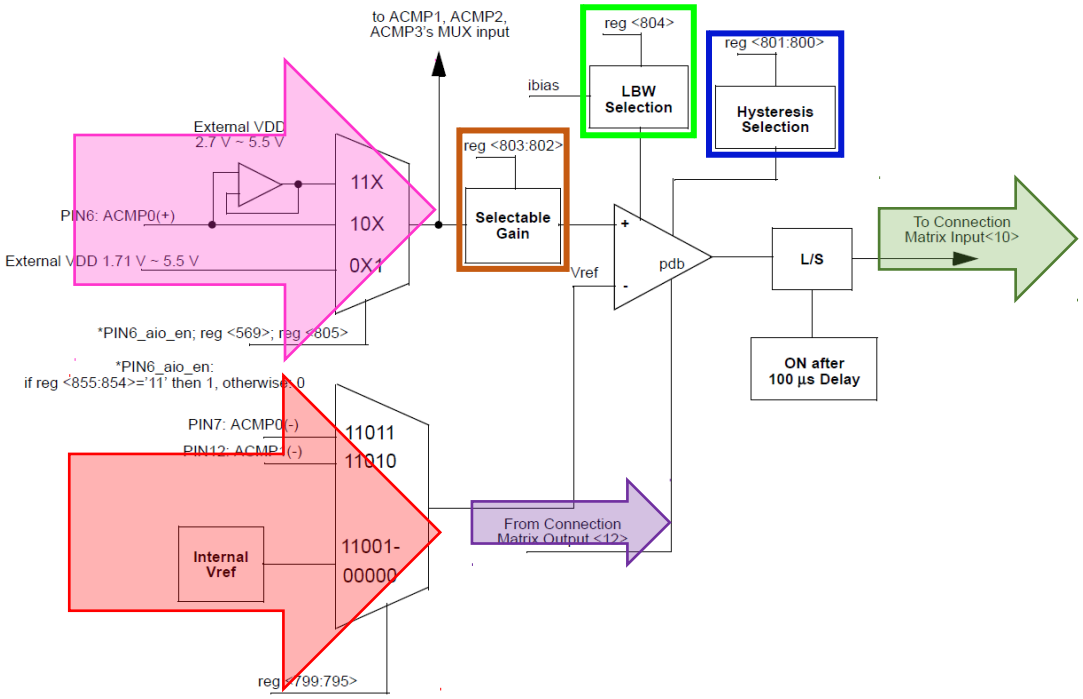
4-Bit LUT or 8- Bit Counter / Delay Macrocells

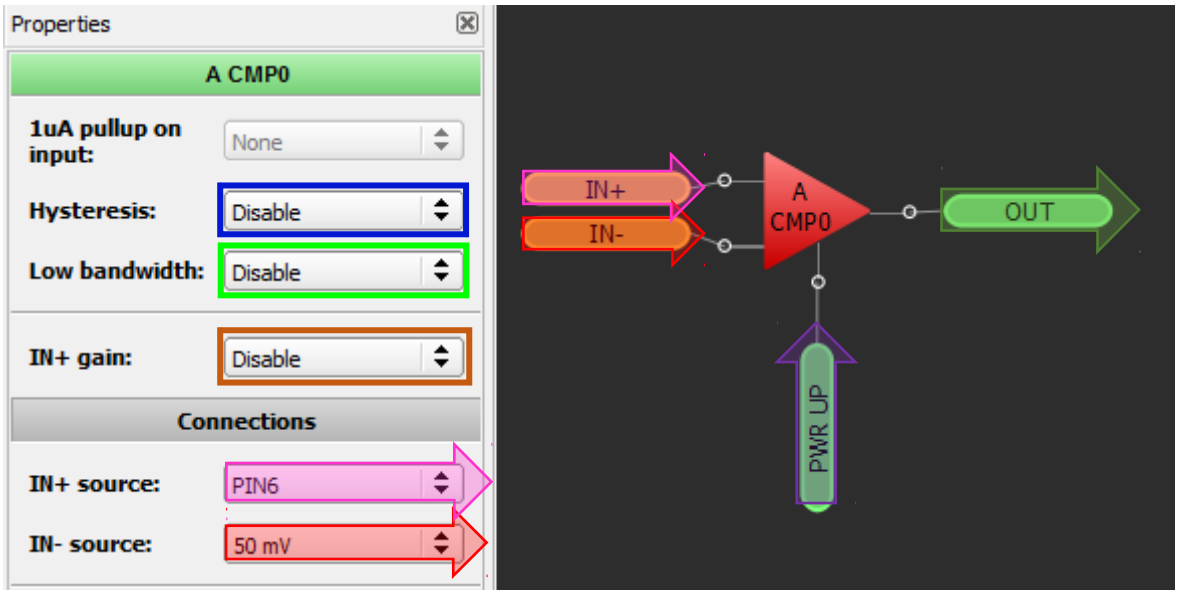



Properties
4-bit LUT0/CNT2/DLY2
Type:
LUT
IN3 IN2 IN1 IN0 OUT
0 0 0 0 0
0 0 0 1 0
0 0 1 0 0
0 0 1 1 0
0 1 0 0 0
0 1 0 1 0
0 1 1 0 0
0 1 1 1 0
1 0 0 0 0
1 0 0 1 0
1 0 1 0 0
1 0 1 1 0
1 1 0 0 0
1 1 0 1 0
1 1 1 0 0
1 1 1 1 0
Standard gates
Defined by user
All to 0
All to 1
IN3
IN2
IN1
IN0
4-bit LUT0
OUT

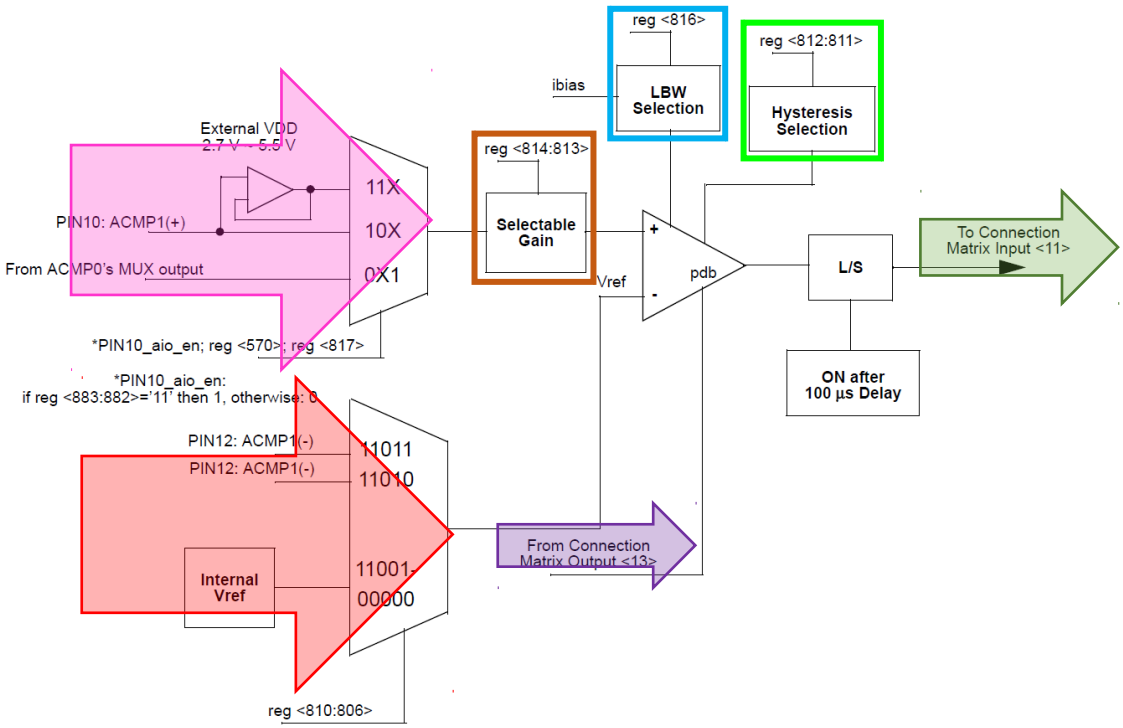

Properties
4-bit LUT0/CNT2/DLY2
Type:
CNT/DLY
Mode:
Delay
Counter data:
1
(Range: 1 - 255)
Delay time:
0.1400 ms
Formula
Edge select:
Both
Connections
Clock:
From RC OSC
Clock source:
RC OSC Freq.
Detailed Info
Apply
CLK
DLY IN
CNT2/DLY2
OUT

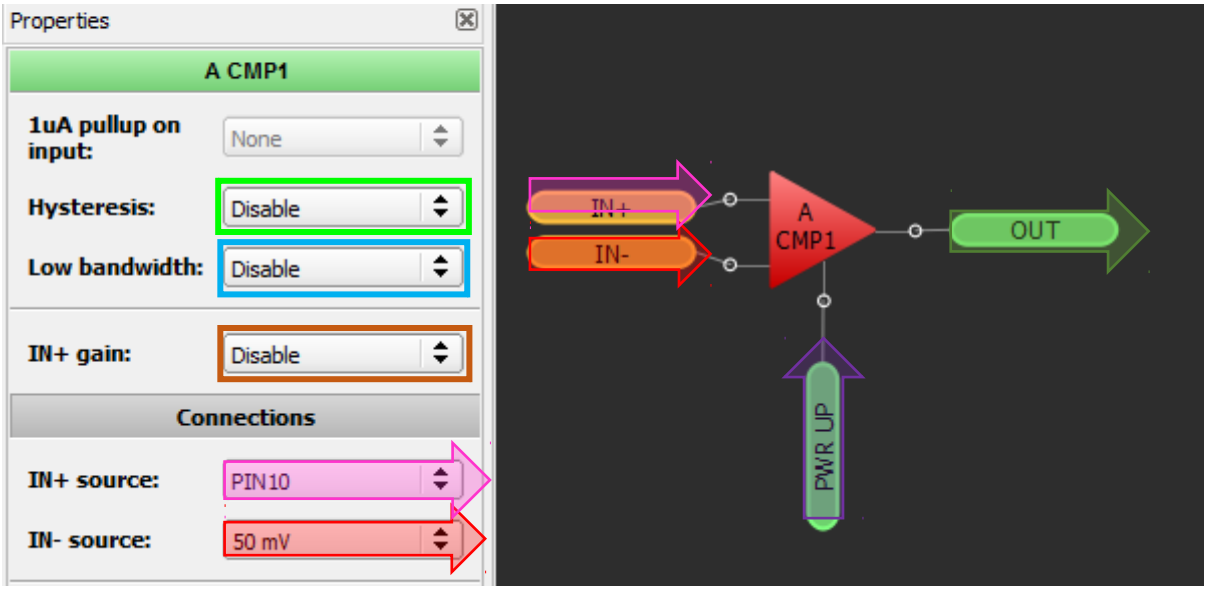
ACMP0 Block Diagram



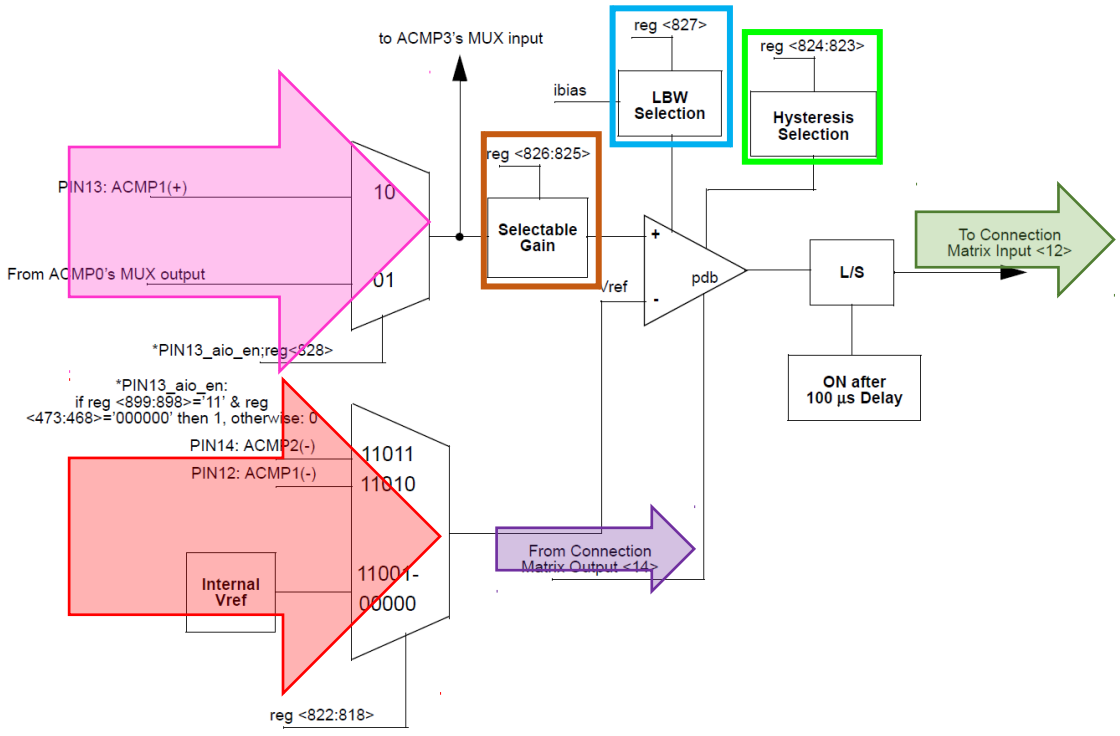


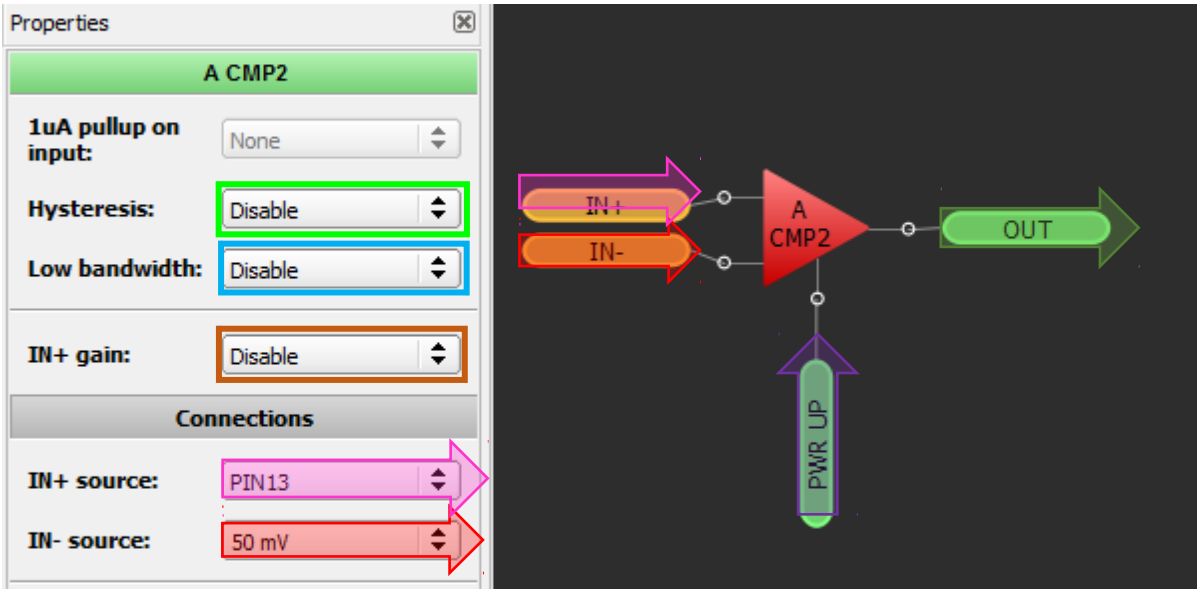
ACMP1 Block Diagram



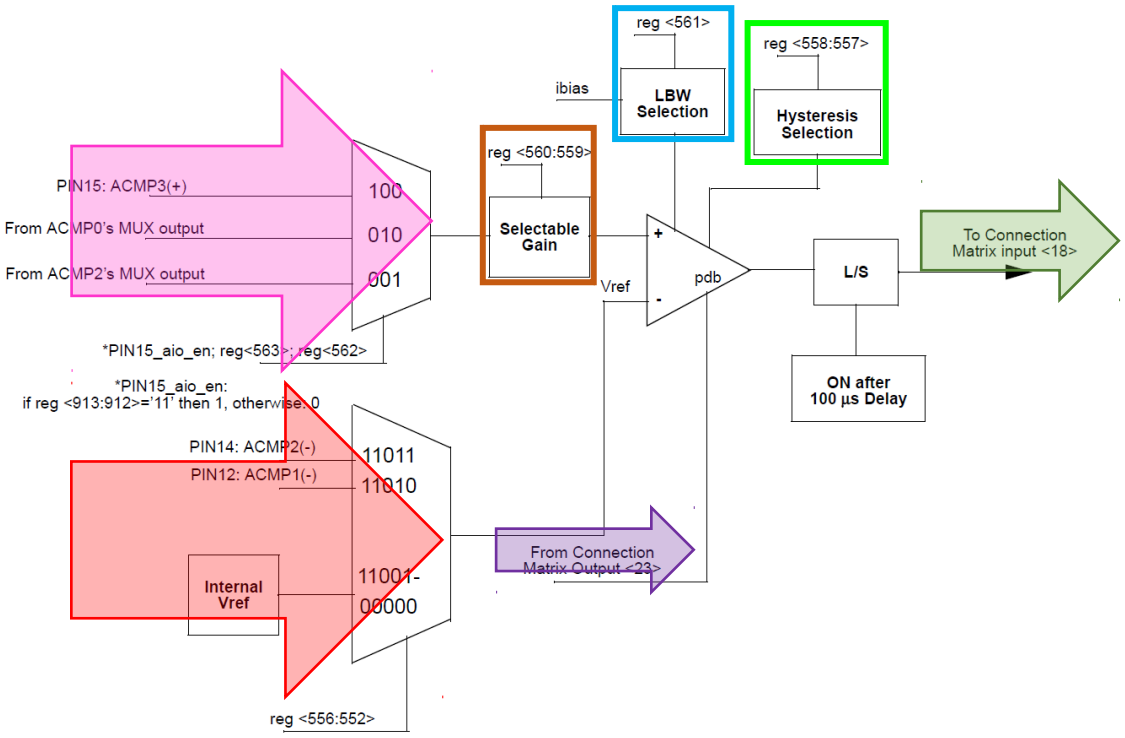


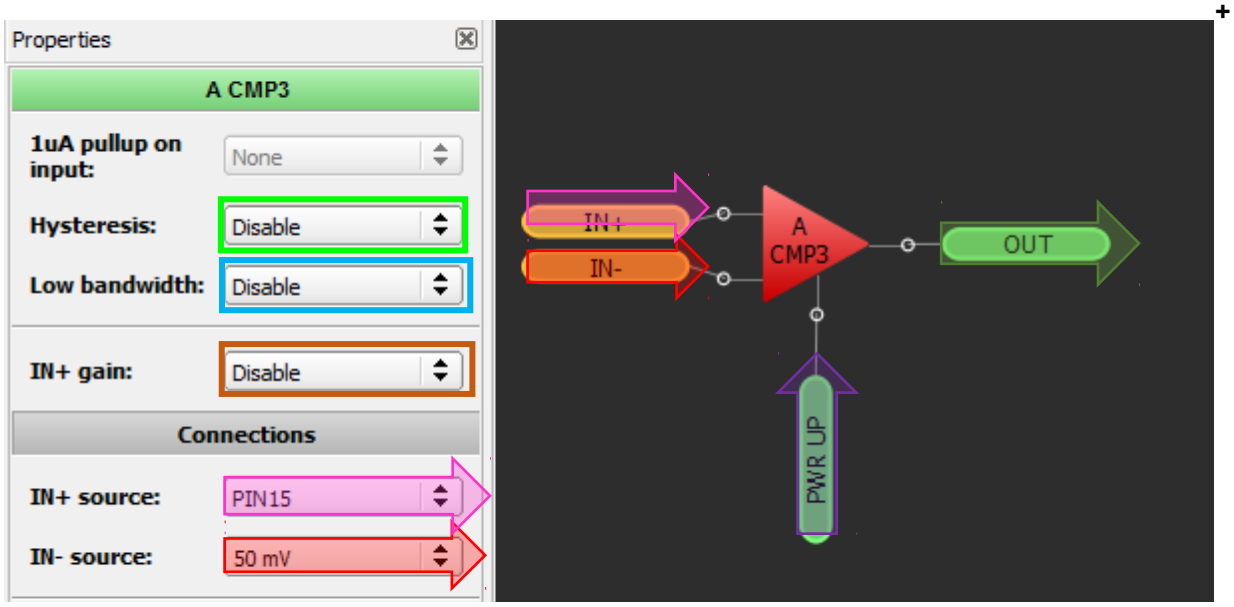
ACMP2 Block Diagram



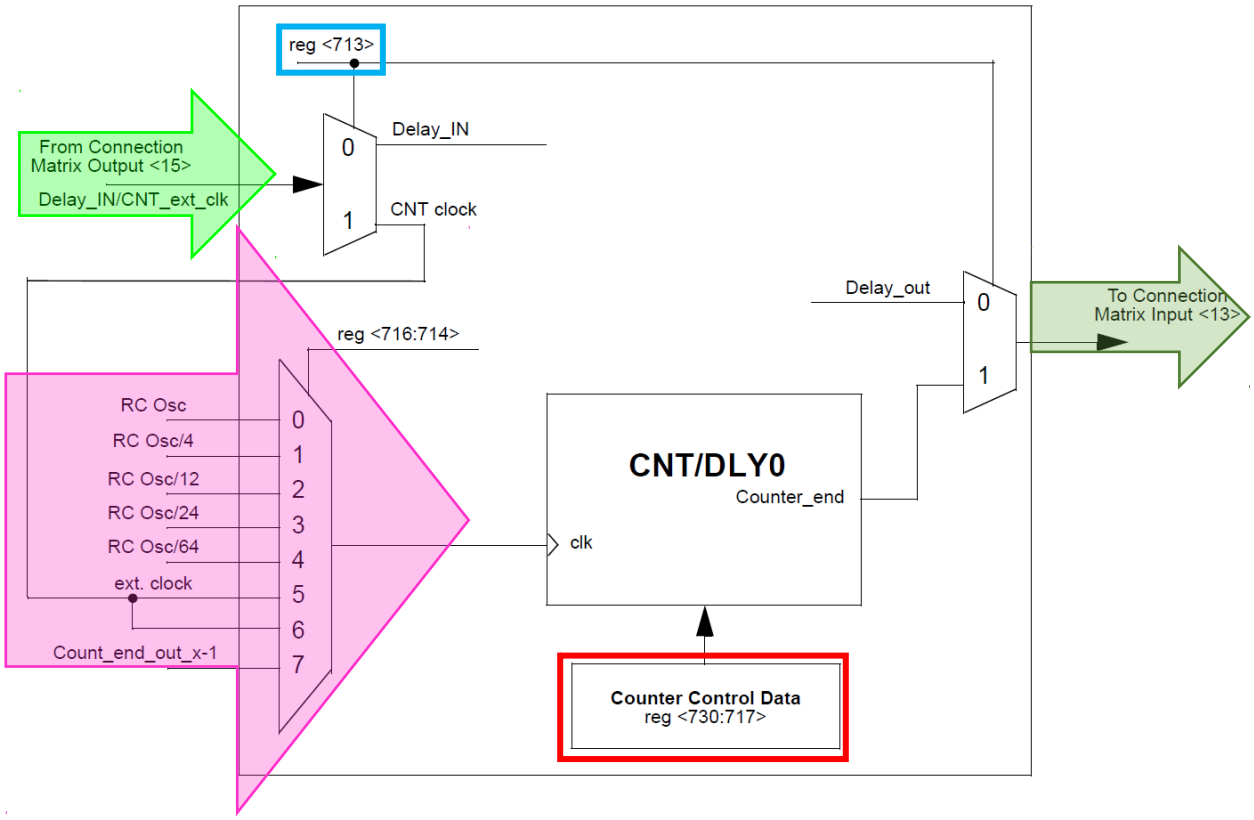


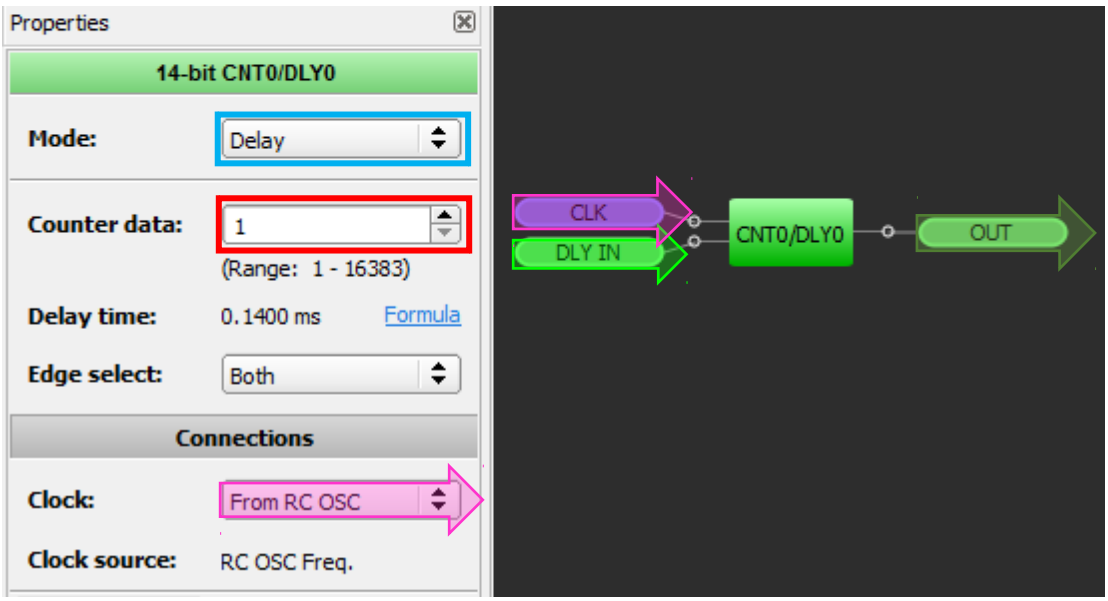
ACMP3 Block Diagram



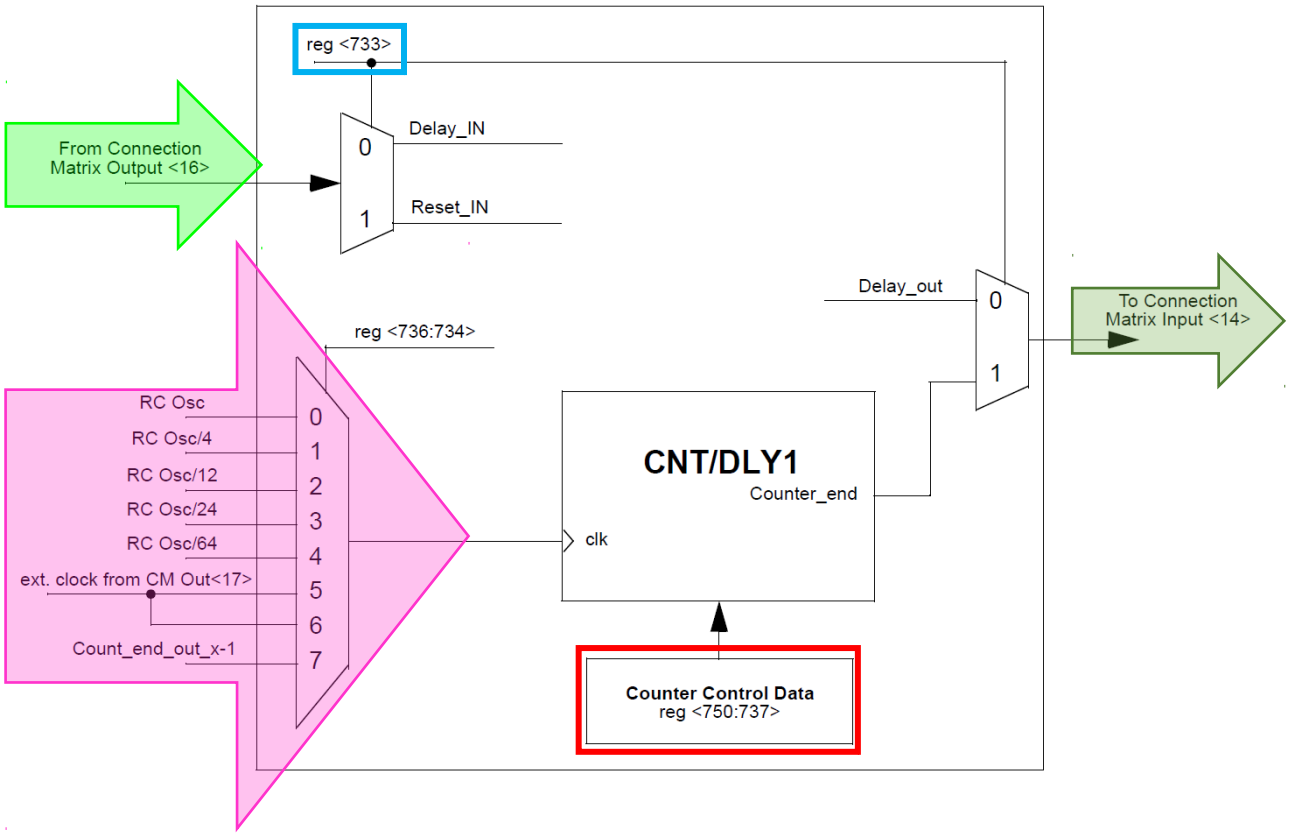


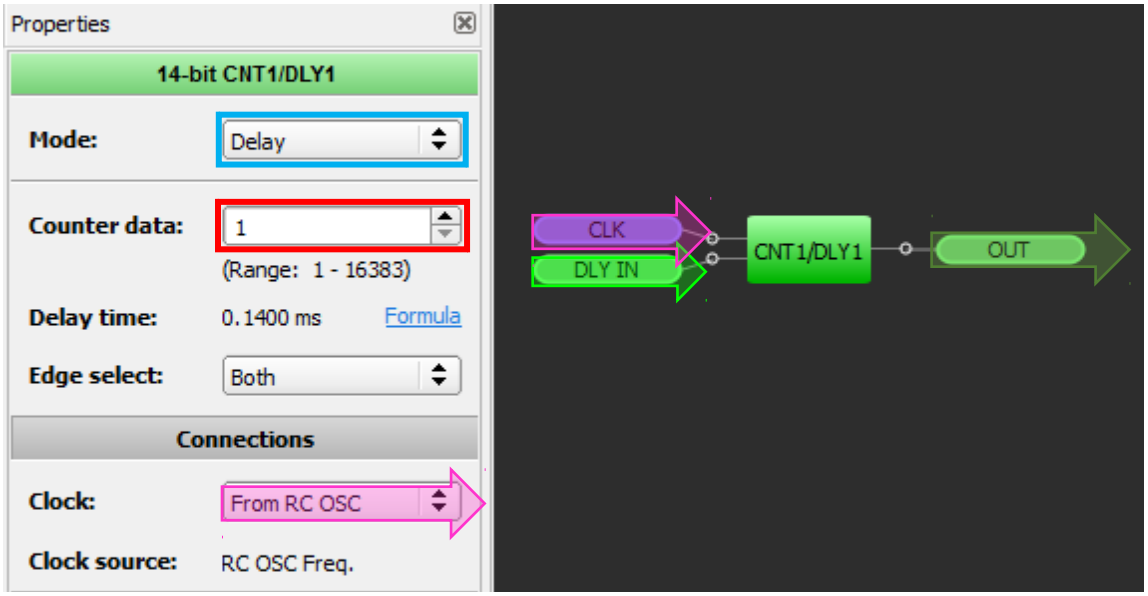
Counters/Delay Generators (CNT/DLY0, 4, 5, 6)



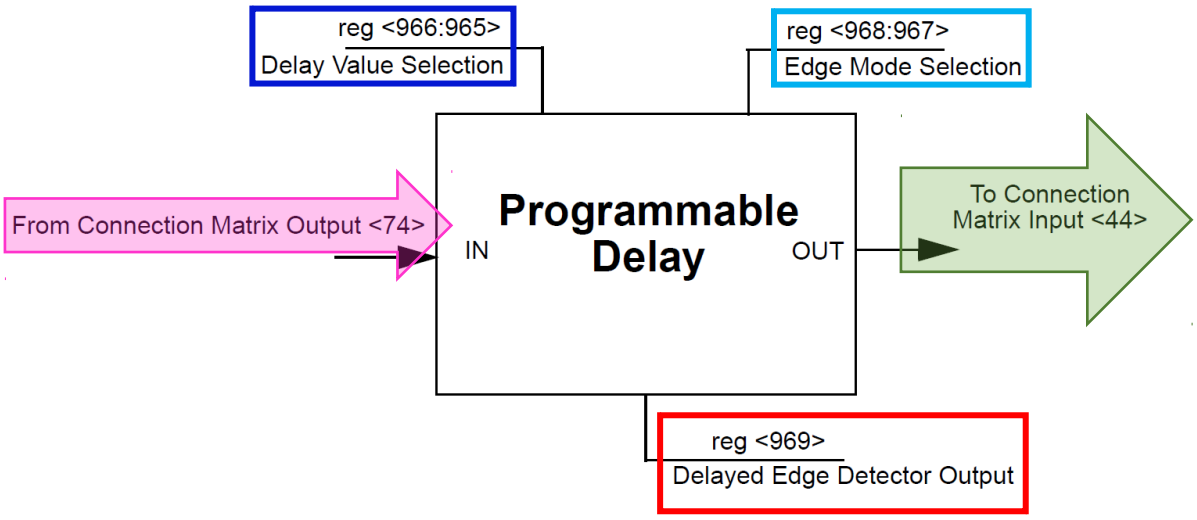


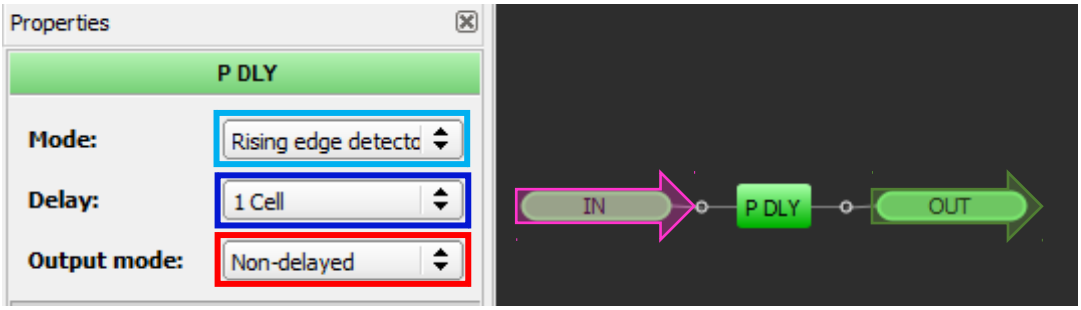
Counters/Delay Generators (CNT/DLY1)



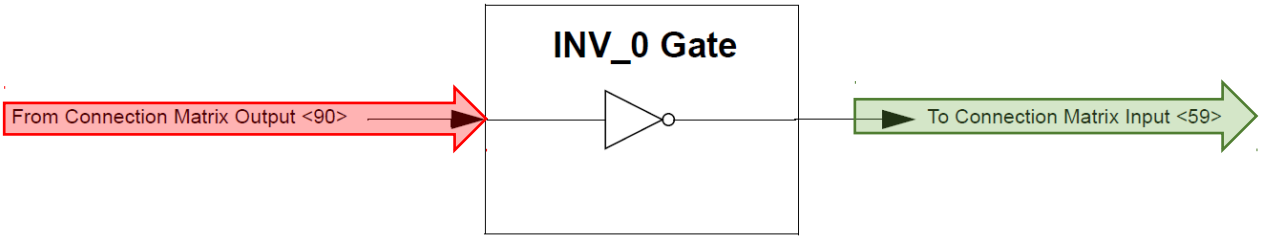


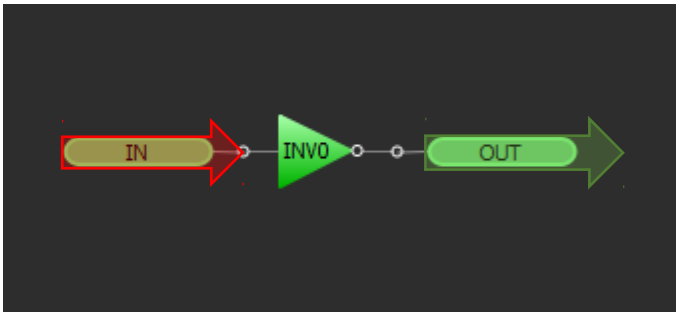
Programmable Delay / Edge Detector



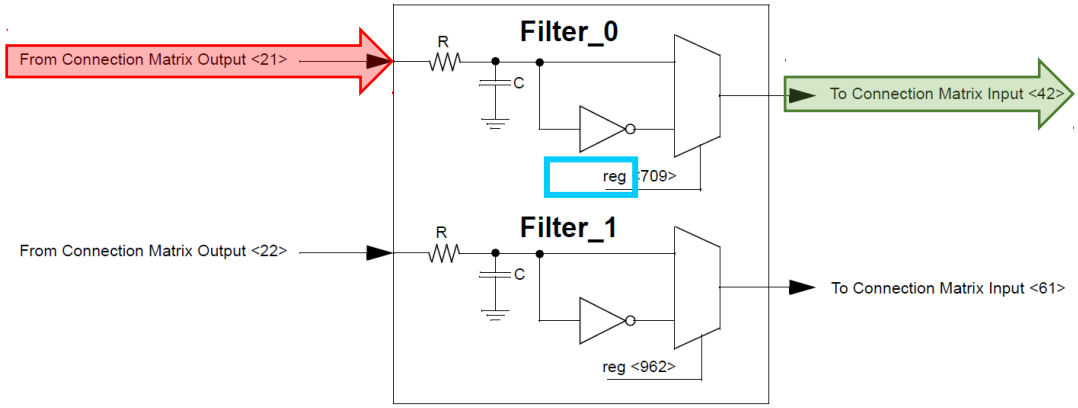


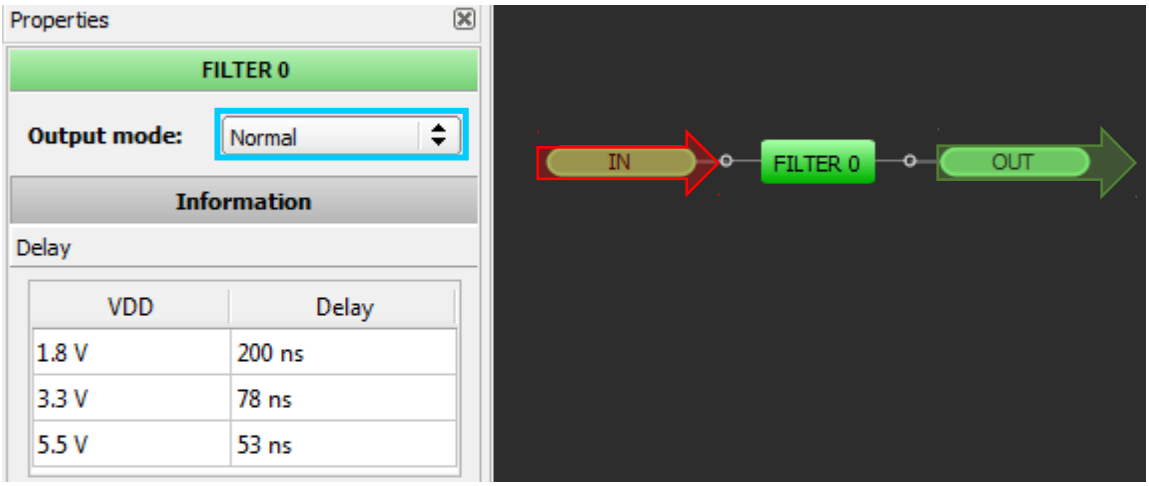
INV 0, INV 1 Gate



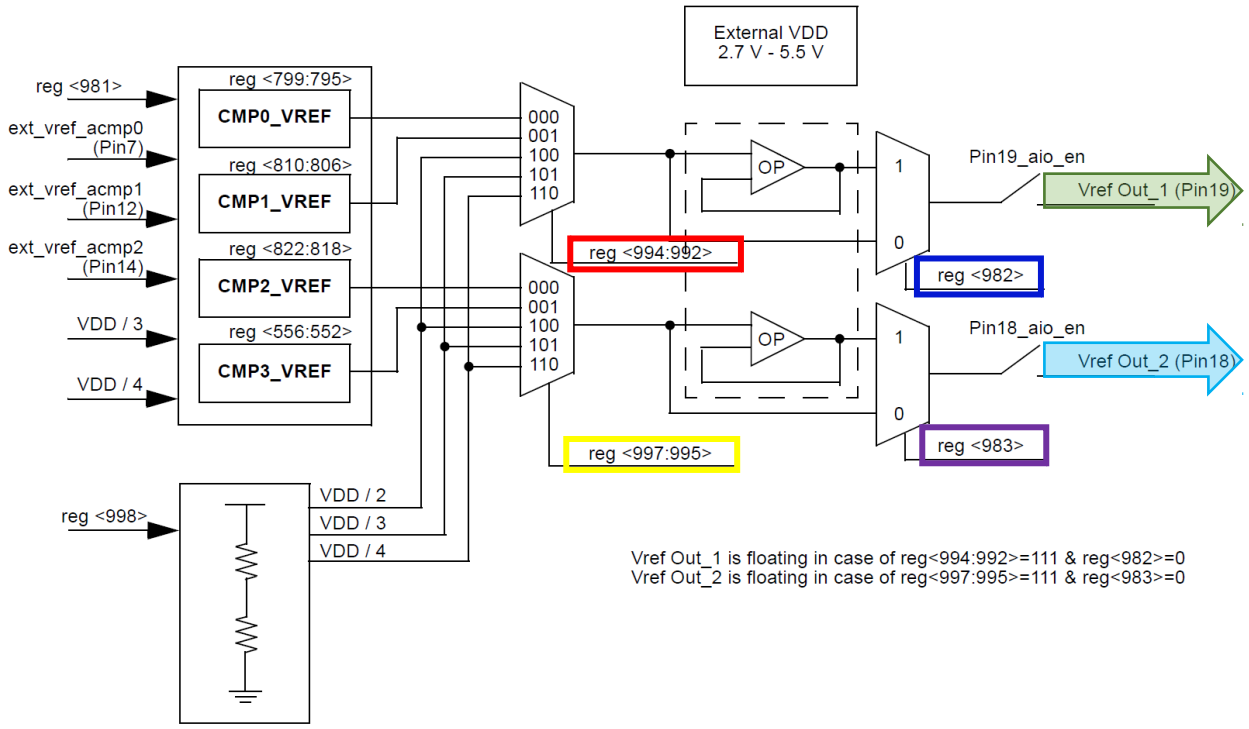


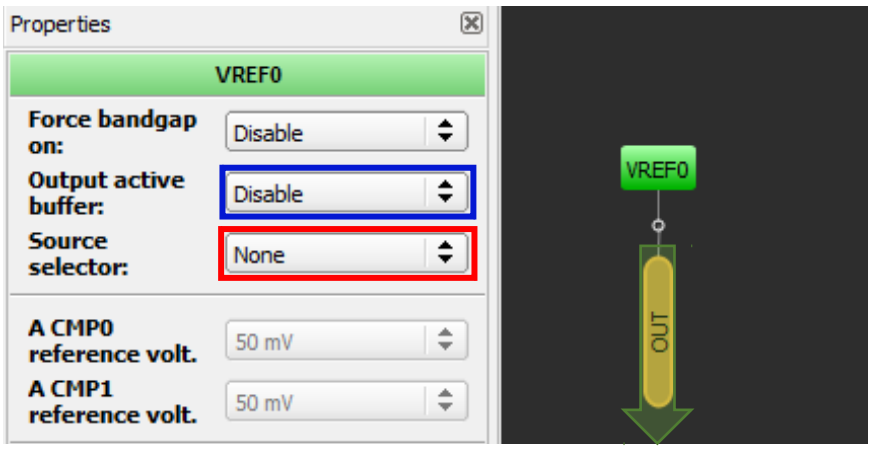
Deglitch Filter

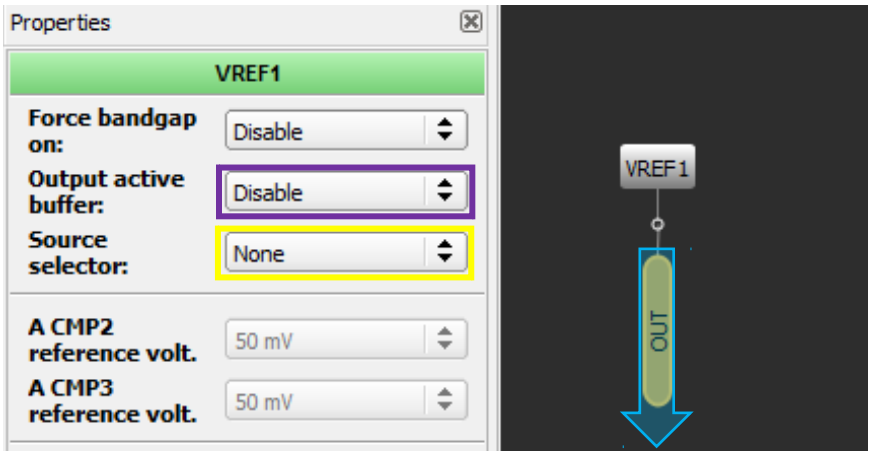




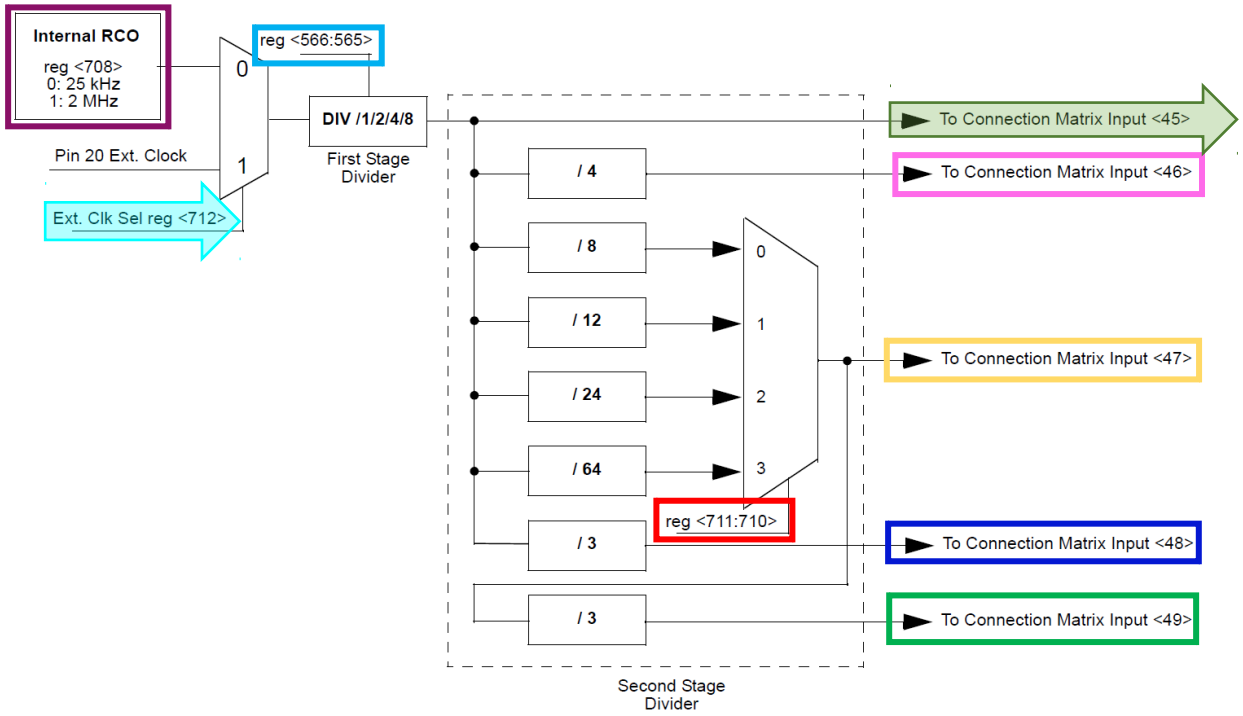
VREF Block Diagram

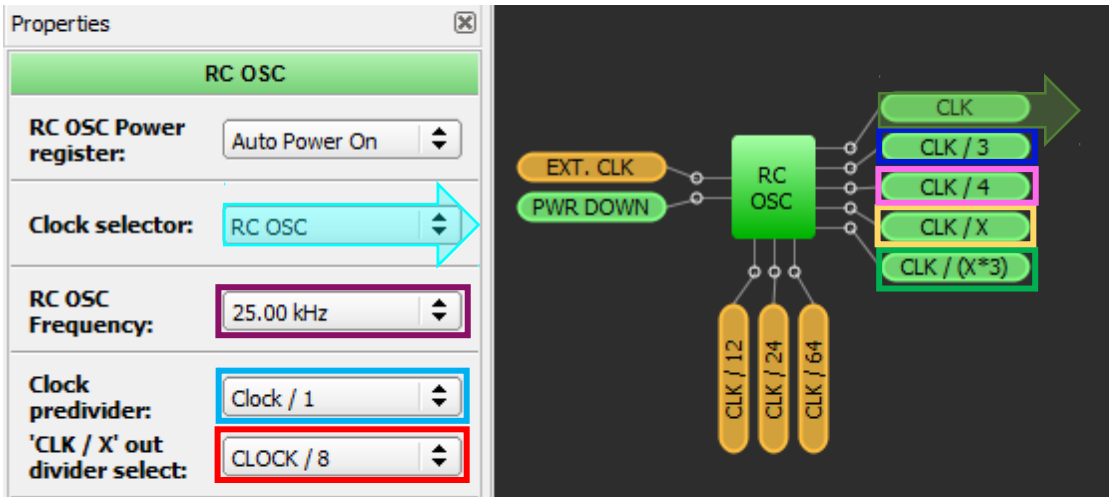





Properties
VREF1
Force bandgap on:
Disable
Output active buffer:
Disable
Source selector:
None
A CMP2 reference volt.
50 mV
A CMP3 reference volt.
50 mV
VREF1
OUT

RC OSC Block Diagram





A. Example projects.

In the GreenPAK Designer **Help** menu, you can find a link to the **Examples** directory. There you can find fully configured examples which can help get your projects completed more quickly. Each example has documentation that contains diagrams and descriptions.